

2024 EOS/ESD Symposium



imec

Toward a Trillion Transistors
ESD Perspectives on Emerging IC Technologies

Marko Simicic

29 October 2024



Marko Simicic

Works at IMEC

Employment location Leuven



imec

Full-time · 7 yrs 2 mos

- **R&D Team Lead**
Aug 2024 - Present · 3 mos
Leuven, Flemish Region, Belgium
- **Principal Member of Technical Staff**
Jul 2024 - Present · 4 mos
Leuven, Flemish Region, Belgium
- **R&D Engineer**
Sep 2017 - Jul 2024 · 6 yrs 11 mos
Kapeldreef 75, 3001 Leuven, Belgium

2012

REPUBLIKA HRVATSKA
SVEUČILIŠTE U ZAGREBU
FAKULTET ELEKTROTEHNIKE I RAČUNARSTVA



Sveučilište u
Zagrebu

DIPLOMA

MARKO SIMIČIĆ

MAGISTAR INŽENJER
ELEKTROTEHNIKE I

INFORMACIJSKE TEHNOLOGIJE



FAKULTET
ELEKTROTEHNIKE
I RAČUNARSTVA

2018

KU LEUVEN



Marko Simicic

Doctor of Engineering Science (PhD)

Electrical Engineering



5,500 employees from more than 100 nationalities



~12,000 m² cleanroom



over 250 tools



System partners

Materials partners

Fabless/FABlite/EDA

Equipment suppliers

IDMs/Foundries

Design houses

over 600 partners



Global collaboration with >200 universities



Long-term research pipeline and fundamental insights



Turning academic insights into industrial innovations



2025 International ESD Workshop (IEW)

Announcement and call for posters

Monday 12 May – Friday 16 May 2025

Hotel Dubrovnik, Gajeva ulica 1, Zagreb, Croatia

Abstract Submission

18 November 2024

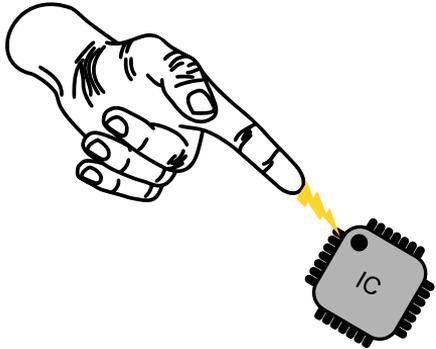
www.esda.org/events/2025-international-esd-workshop-iew-europe



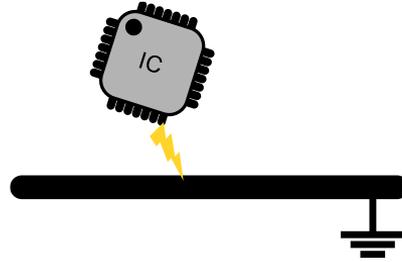
ElectroStatic Discharge (ESD)

A sudden flow of electricity
between two electrically
charged objects

A person touches a device
Human Body Model (HBM)



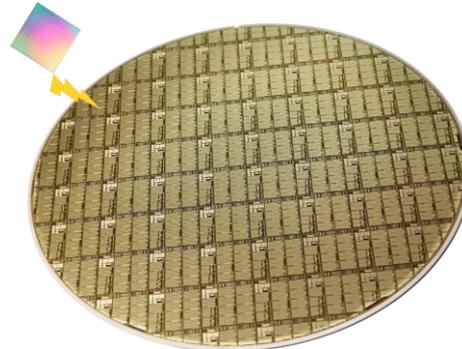
A device touches a conductor
Charged Device Model (CDM)



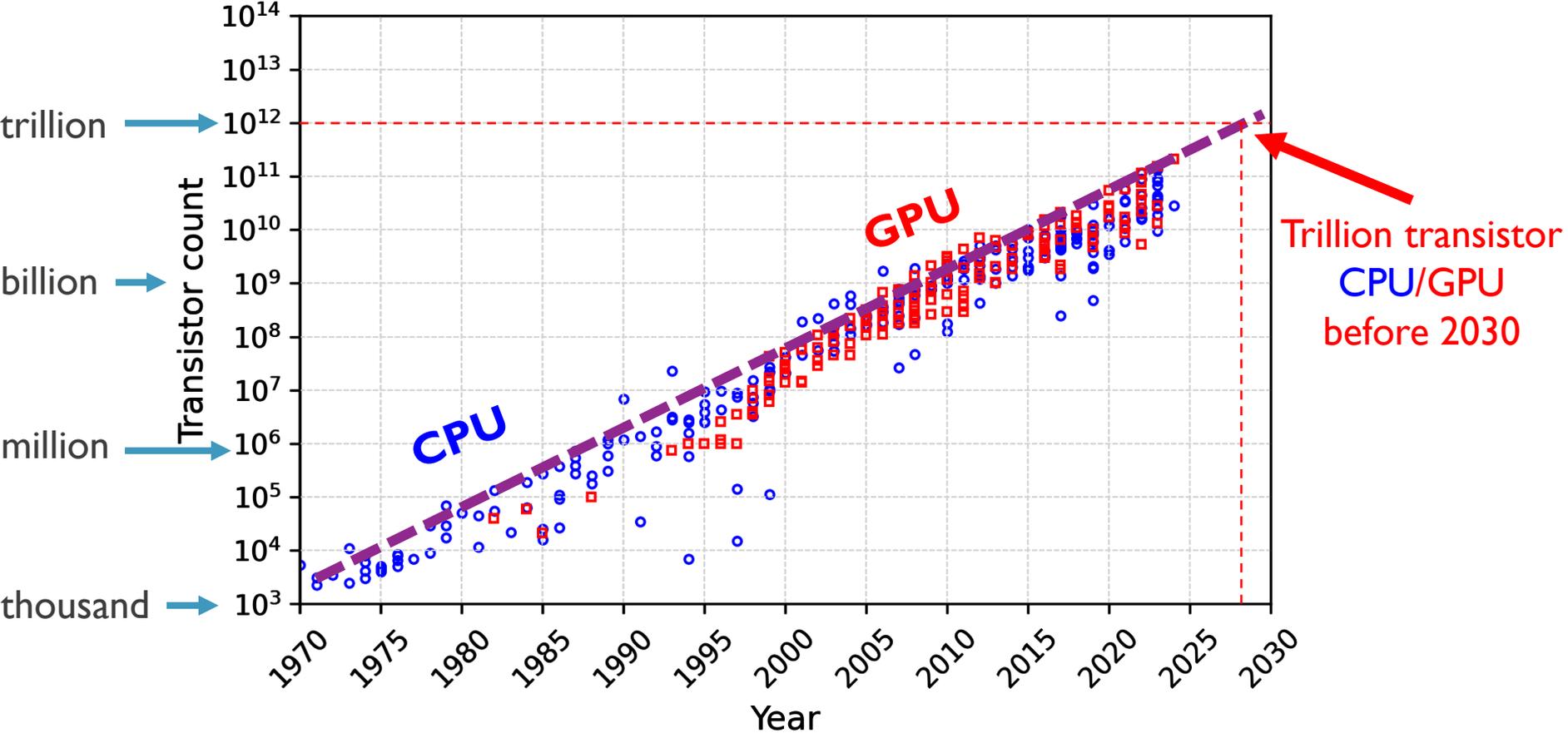
What about chiplets?

No standard yet, but...

Charged Chiplet Model ? (CCM)

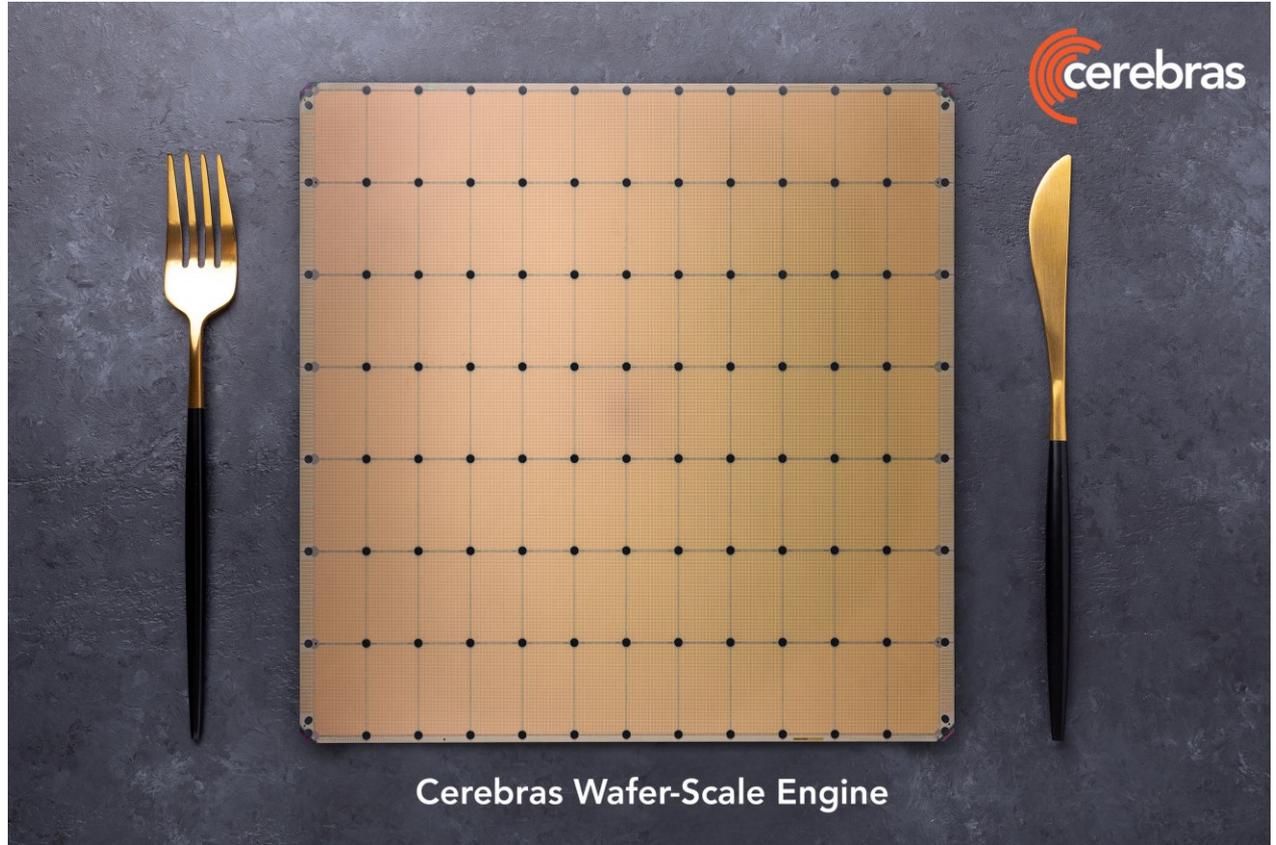


Every semiconductor presentation has to start with... Moore's Law



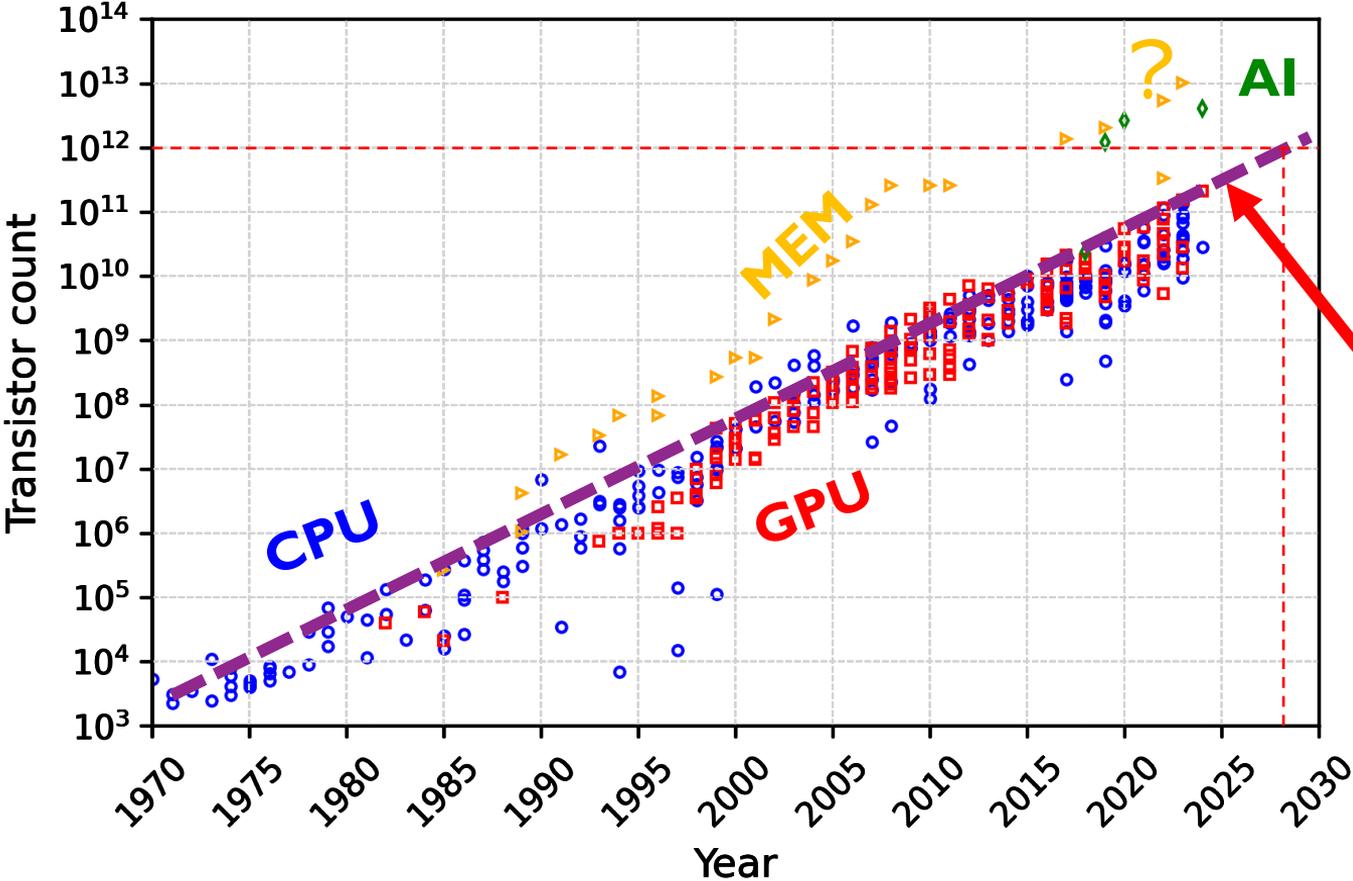
Except... Cerebras – 4 trillion transistors – August 2024

- 3rd generation Wafer Scale Engine
- 46 225 mm²
- 900 000 compute cores
- 44 GB on-chip memory
- TSMC 5nm technology



“Cerebras Systems Unveils the Industry’s First Trillion Transistor Chip”, <https://www.cerebras.net/press-release/cerebras-systems-unveils-the-industrys-first-trillion-transistor-chip/>, accessed 18 August 2024

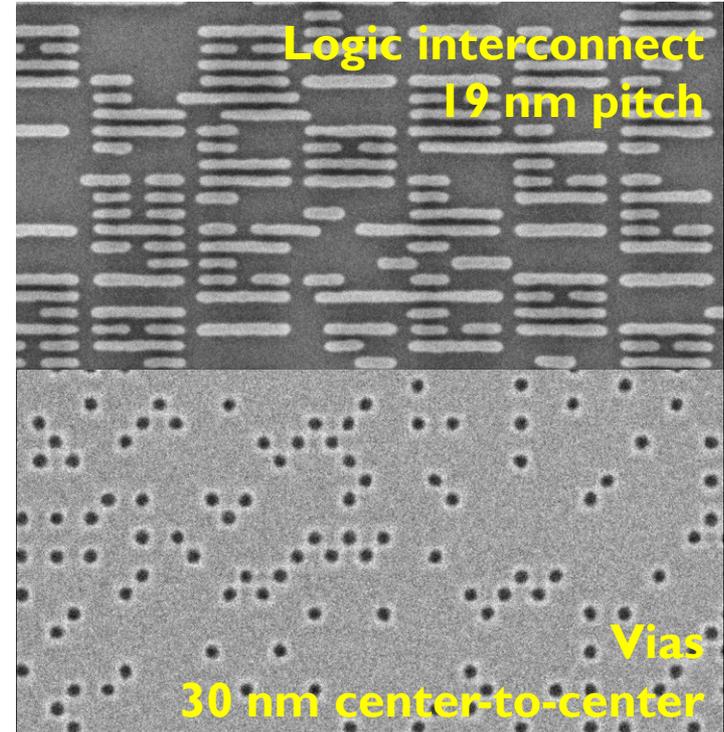
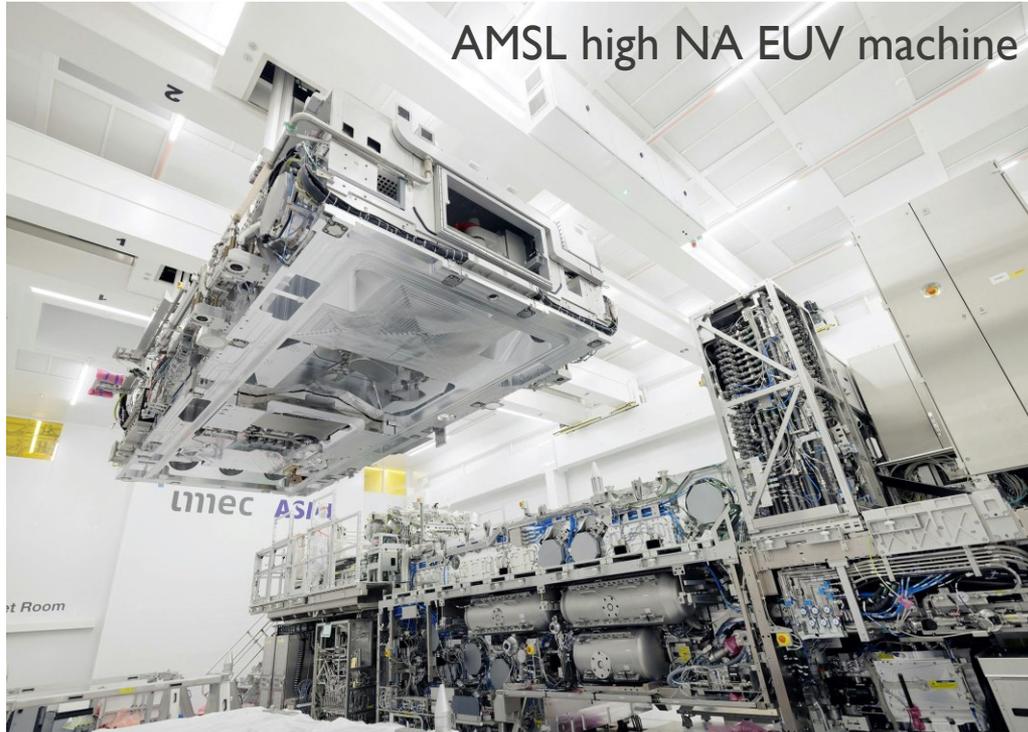
Memory and some AI cores are beyond Moore's scaling



How will this continue?

What can we expect?

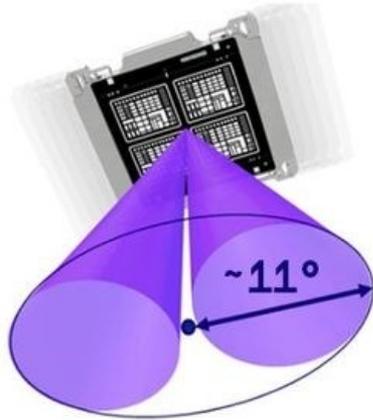
High Numerical Aperture (NA) Extreme-UV (EUV) Lithography



- Imec press release, "Imec and ASML open joint High NA EUV Lithography Lab offering an early development platform to the leading-edge semiconductor ecosystem", 3 June 2024, <https://www.imec-int.com/en/press/asml-and-imec-open-joint-high-na-euv-lithography-lab-offering-early-development-platform>, accessed: 18 August 2024.
- Imec press release, "Imec demonstrates logic and DRAM structures using High NA EUV Lithography", 7 August 2024, <https://www.imec-int.com/en/press/asml-and-imec-open-joint-high-na-euv-lithography-lab-offering-early-development-platform>, accessed: 18 August 2024.

Lithography field (reticle) size limits the number of transistors on a monolithic die

EUV today
0.33 NA

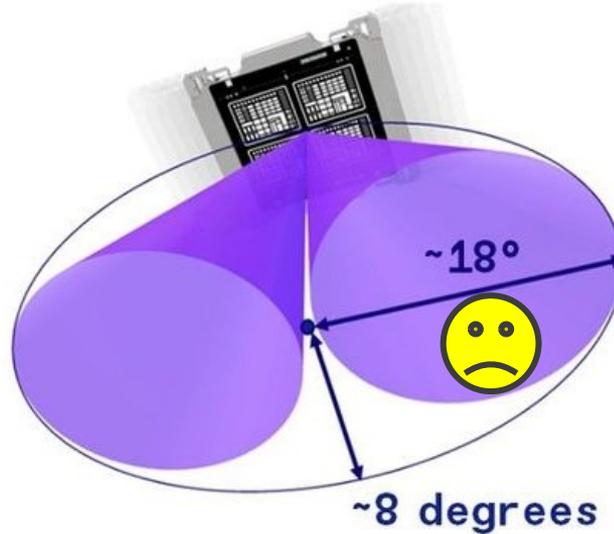


EUV today

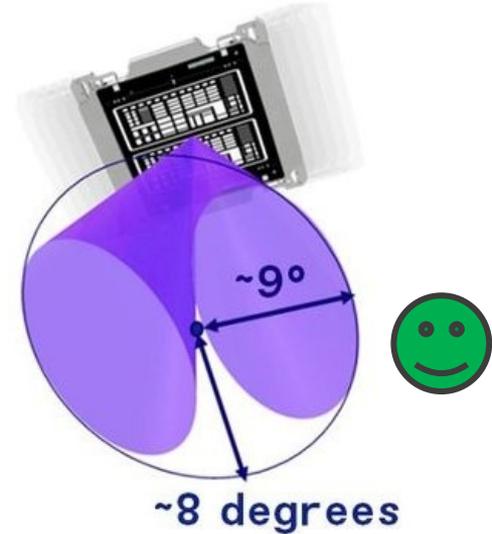
Field size: 26 x 33 mm

Maximum single-exposure
monolithic chip **size: 858 mm²**

Reflection angle is too wide!
0.55 NA



EUV tomorrow
0.55 NA

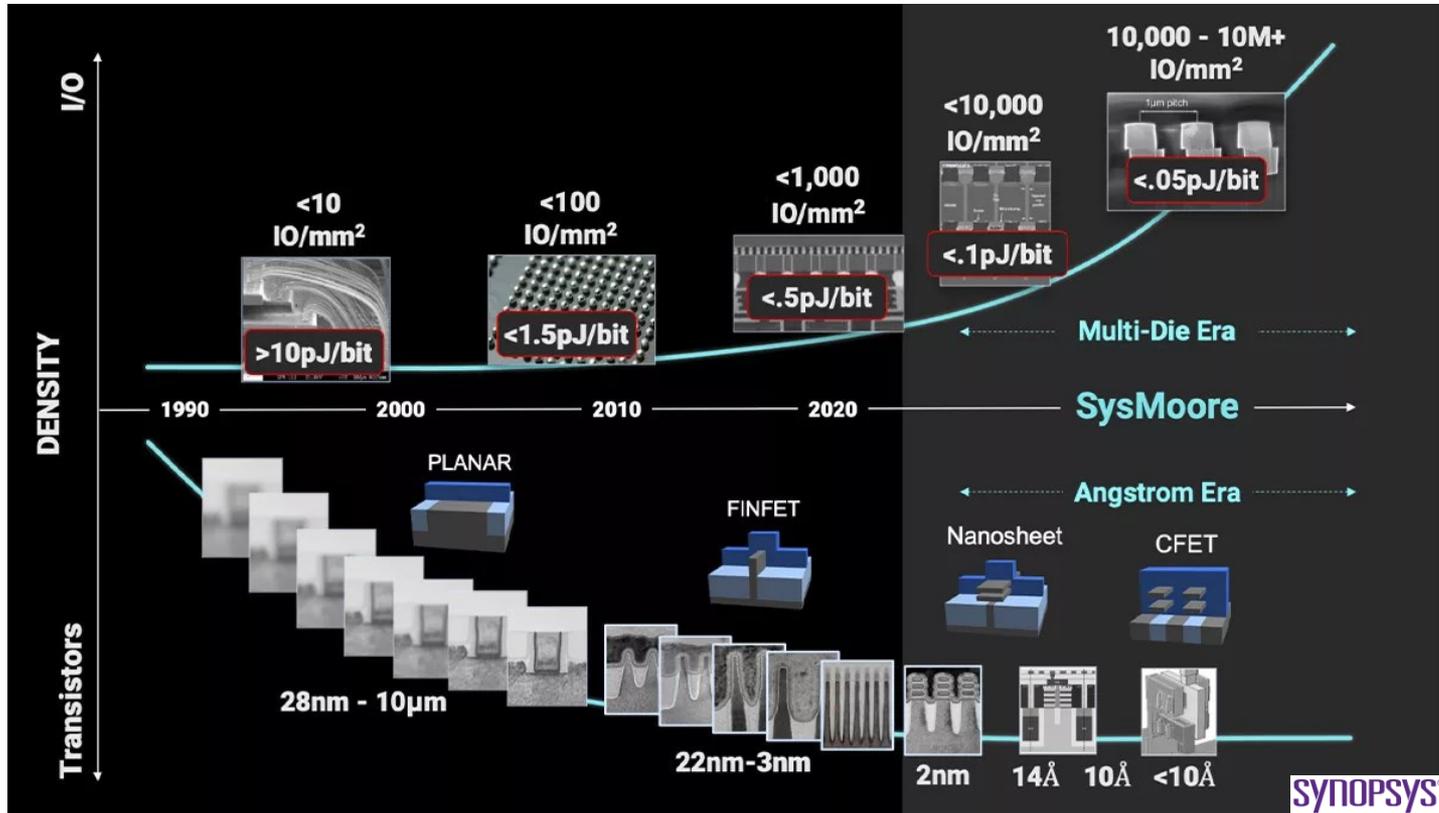


EUV tomorrow

Field size: 26 x 16.5 mm

Maximum single-exposure
monolithic **chip size: 429 mm²**

Multi-die (chiplet) systems will continue Moore's law

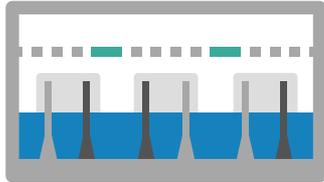


Aart de Geus, "Chapter I: SysMoore – Systemic Complexity with a Moore's Law Ambition!", <https://www.synopsys.com/multi-die-system/how-multi-die-systems-will-change-semiconductor-design.html>, accessed 20/10/2023

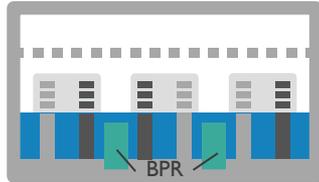
Logic device roadmap

Logic Scaling Roadmap

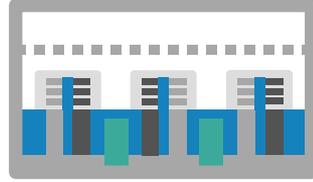
Standard cell evolution enabled by new device architectures



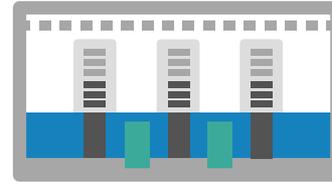
FinFET
5T



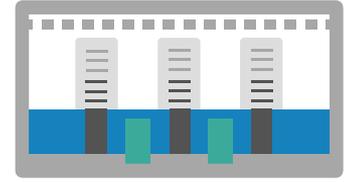
Nanosheets, BPR
5T



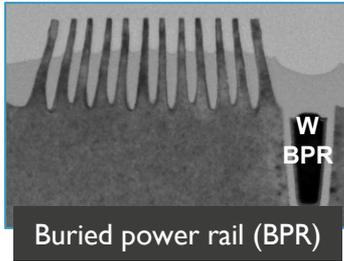
Forksheets, VHV std cell arch.
<5T



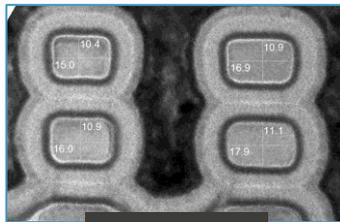
CFET, BEOL w/ airgaps
4T



2D atomic channels
<4T



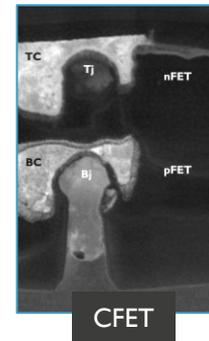
Buried power rail (BPR)



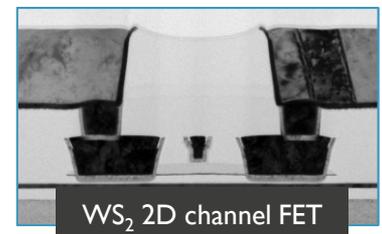
Nanosheets



Forksheets



CFET



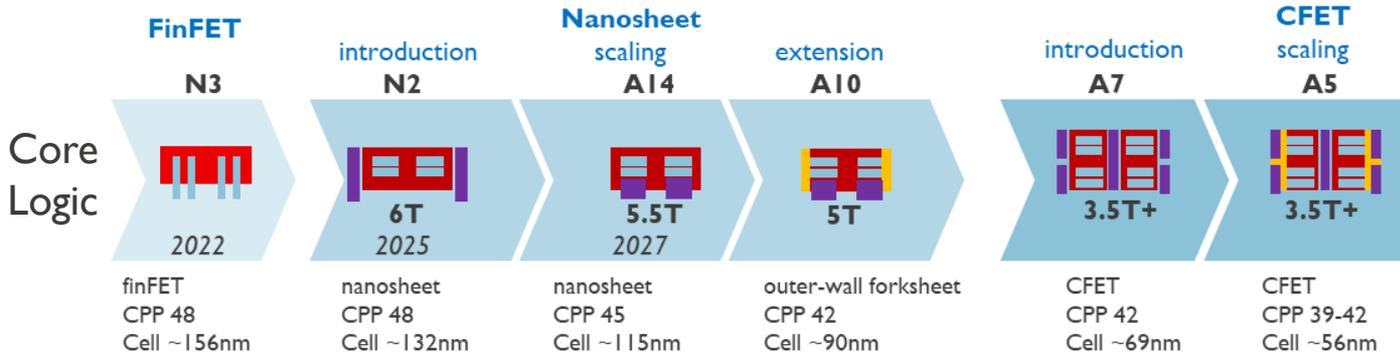
WS₂ 2D channel FET

PP: poly pitch (nm)

MP: dense metal pitch (nm)

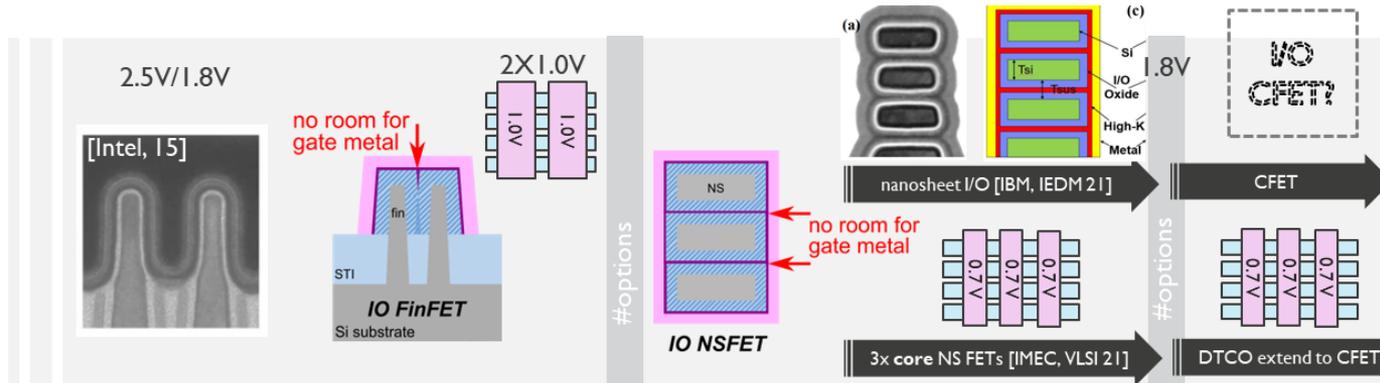
CFET: Complementary FET

Thick-oxide transistors more challenging in new technologies



Thick-oxide I/Os

- 2...3xVDD simple inverter

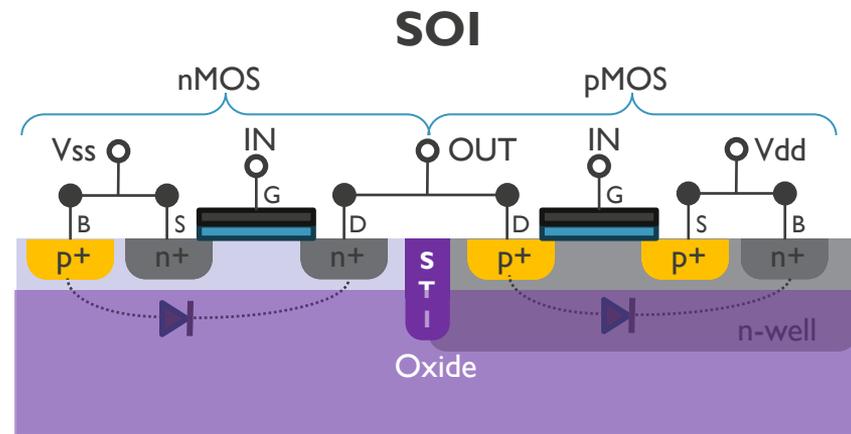
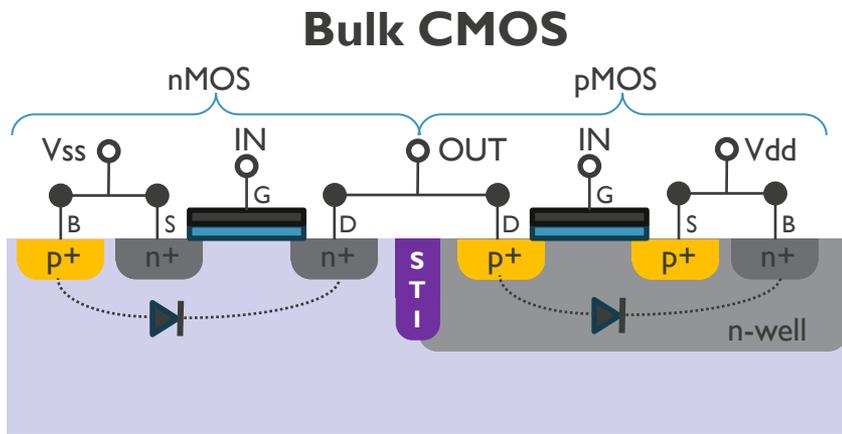


Core-transistor I/Os

- 2...3xVDD I/O made of stacked core transistors

Wen-Chieh Chen et al., "A 1.8V GPIO with Design-Technology-Reliability Co-Optimization in Sub-3nm GAA-NS Technology", JSSC, 2024. [CFET]: J. Ryckaert et al., "The Complementary FET (CFET) for CMOS scaling beyond N3," in 2018 IEEE Symposium on VLSI Technology, doi: [10.1109/VLSIT.2018.8510618](https://doi.org/10.1109/VLSIT.2018.8510618) [Intel I5] - C.-H. Jan et al., "A 14 nm SoC platform technology featuring 2nd generation Tri-Gate transistors, 70 nm gate pitch, 52 nm metal pitch, and 0.0499 μm^2 SRAM cells, optimized for low power, high performance and high density SoC products." 2015 VLSI Symposium [imec VLSI 21] - Hellings, Geert, et al. "Si/SiGe superlattice I/O FinFETs in a vertically-stacked gate-all-around horizontal nanowire technology." 2018 VLSI Symposium, 2018. [IBM, IEDM 21] - Bhuiyan, Maruf, et al. "Gate-Last I/O transistors based on stacked gate-all-around nanosheet architecture for advanced logic technologies." 2021 IEDM, 2021.

Si bulk is disappearing – FET self-protection is reducing

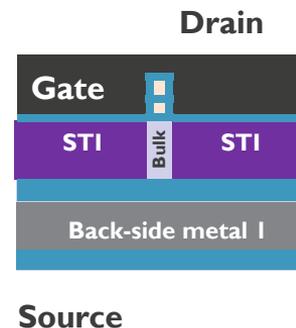
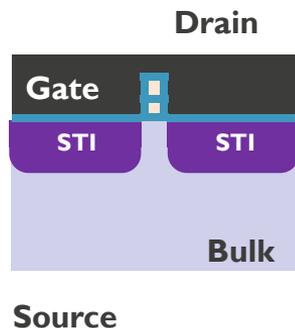
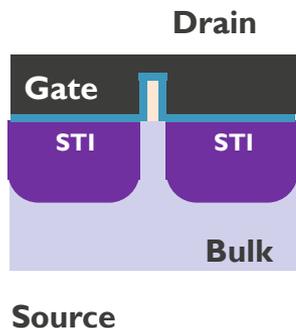
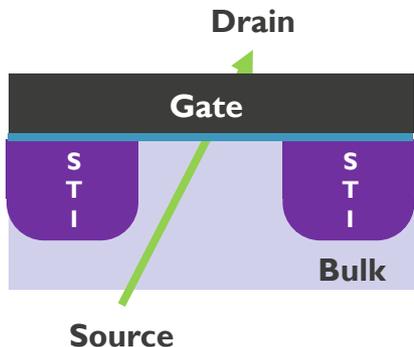


Bulk CMOS

FinFET

GAA

BSPDN



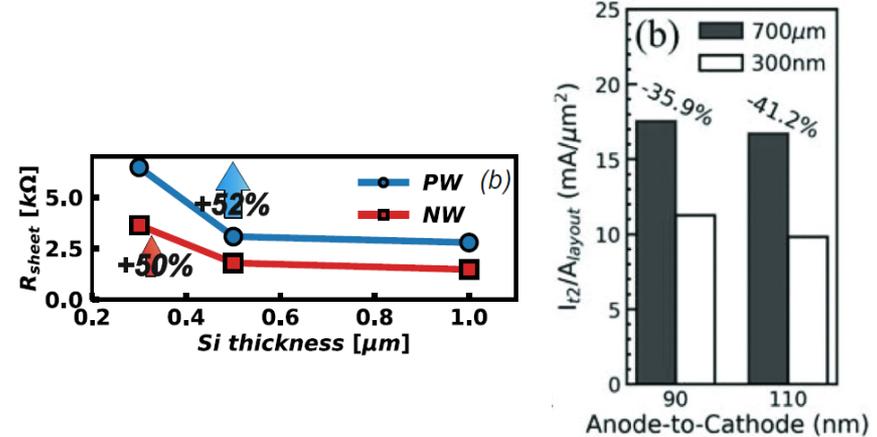
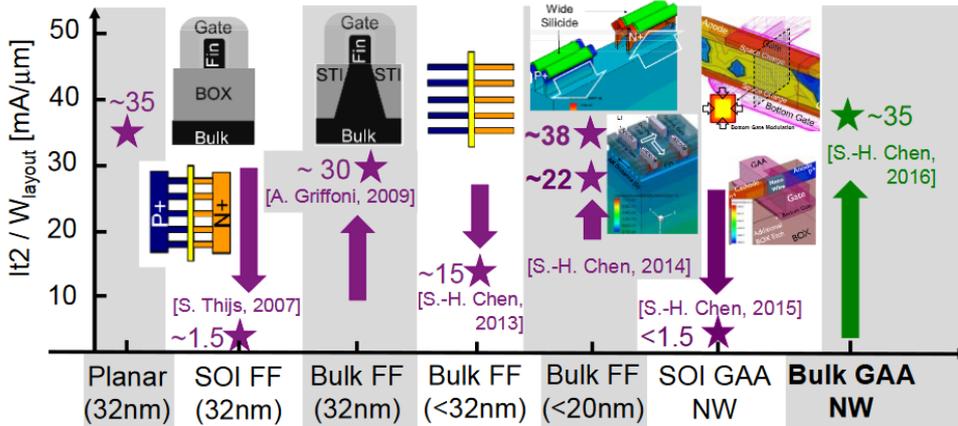
No bulk, but functional backside!

Diode performance is not improving

Planar technologies are better for ESD protection

- Technologies scale
- Diode ESD performance does not scale up

- BSPDN and wafer thinning
- Diode performance is reduced



- Increased resistance = lower ESD performance

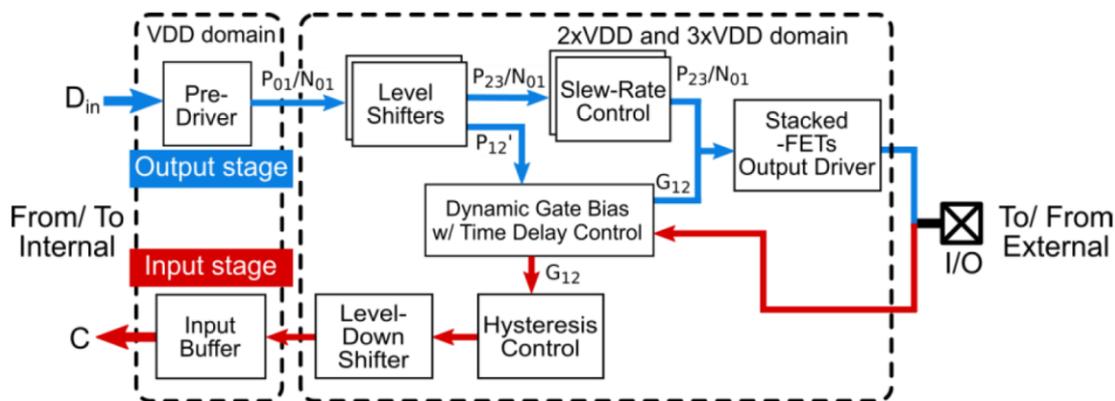
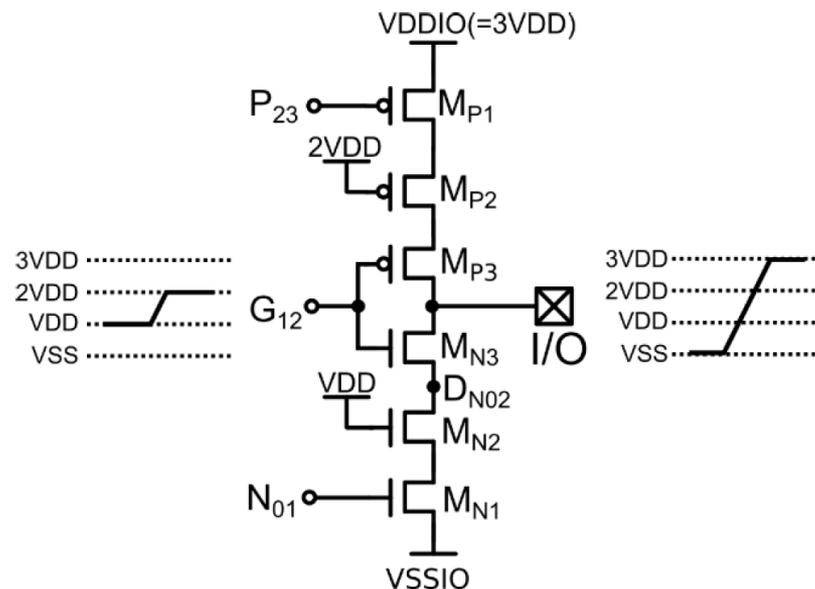
S.-H. Chen et al., "vTLP characteristics of ESD diodes in bulk si gate-all-around vertically stacked horizontal nanowire technology," in 2017 EOS/ESD Symposium. doi: [10.23919/EOS/ESD.2017.8073454](https://doi.org/10.23919/EOS/ESD.2017.8073454).

Left: K. Serbulova et al., "Impact of Sub-μm Wafer Thinning on Latch-up Risk in STCO Scaling Era," EOS/ESD Symposium, 2021. doi: [10.23919/EOS/ESD52038.2021.9574787](https://doi.org/10.23919/EOS/ESD52038.2021.9574787).

Right: W.-C. Chen et al., "ESD Challenges in 300nm Si Substrate of DTCO/STCO Scaling Options," IEDM 2023. doi: [10.1109/IEDM45741.2023.10413663](https://doi.org/10.1109/IEDM45741.2023.10413663).

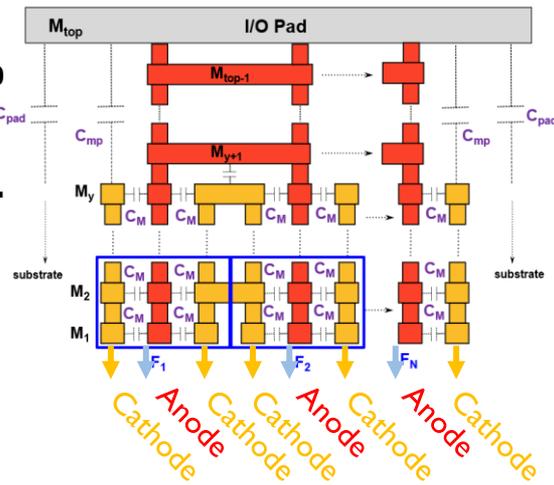
3xVDD general-purpose I/O made with core transistors

- ~1.25x area penalty compared to thick-oxide equivalent (16nm FinFET) (this is w/o ESD layout)
- Including drain ballasting – no penalty!
- Dynamic bias needed to avoid overstress
- GAA → no thick oxide, core I/O only solution

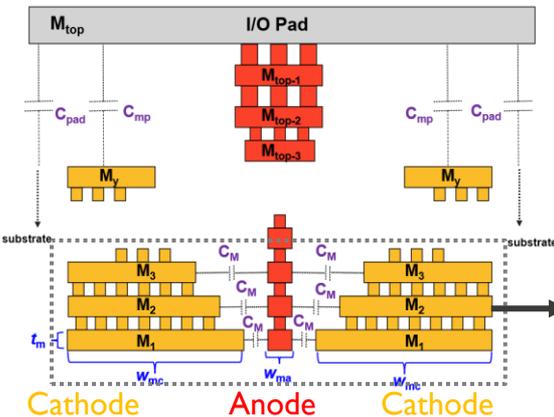


Tapered full-metal lines can improve both RF & ESD performance

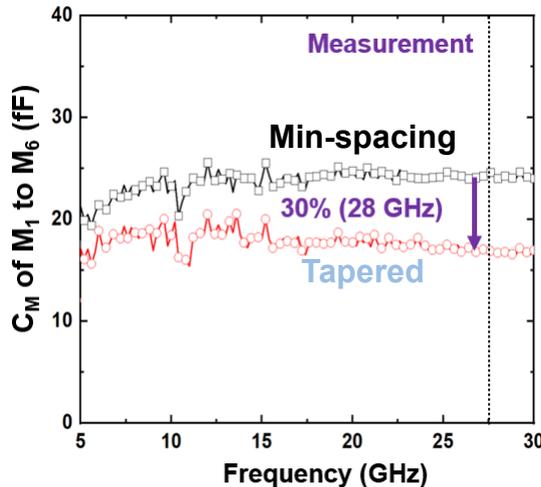
Min-spacing



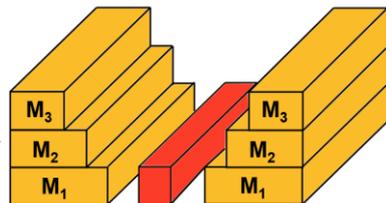
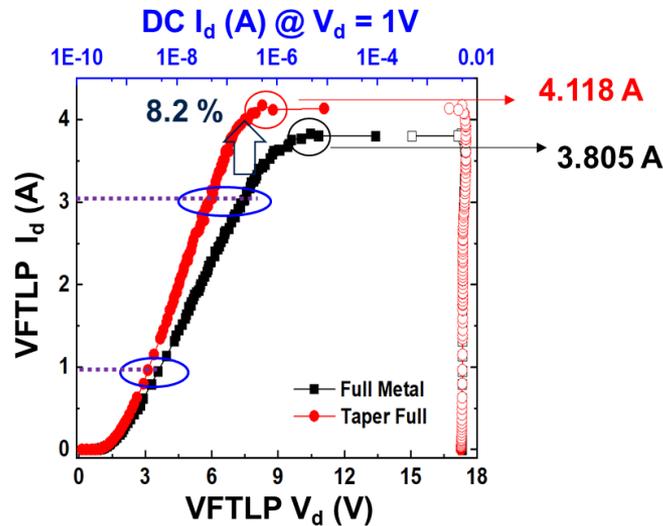
Tapered



Better RF performance!



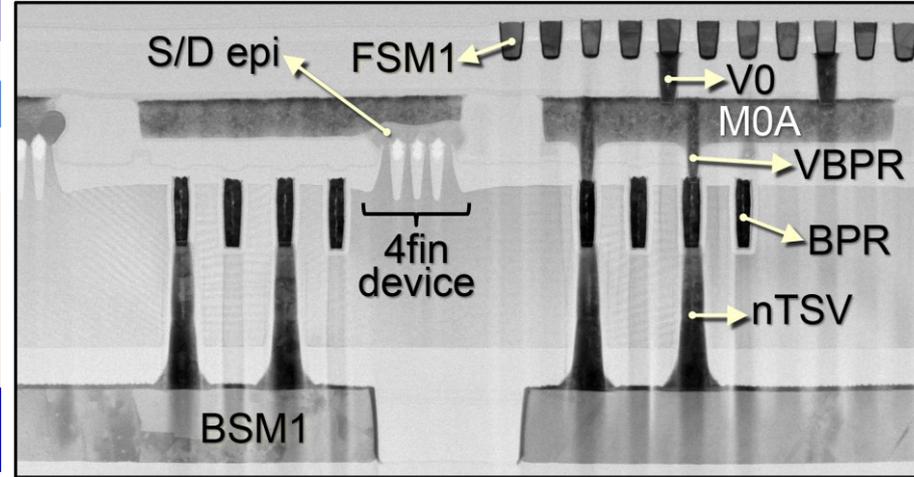
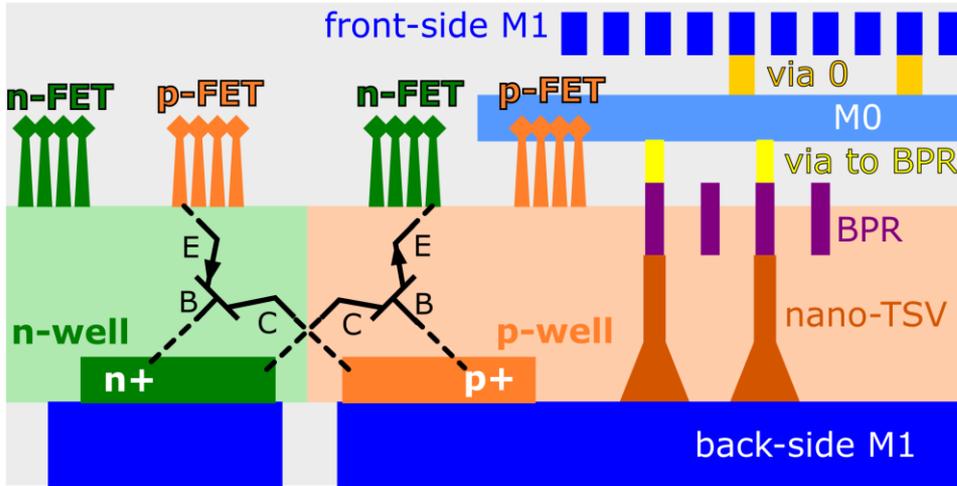
Improved VFTLP robustness!



Technology: 28nm CMOS
Target application: RF/High-Speed I/O

Utilizing the chip backside

Backside contacts are very exciting option for ESD



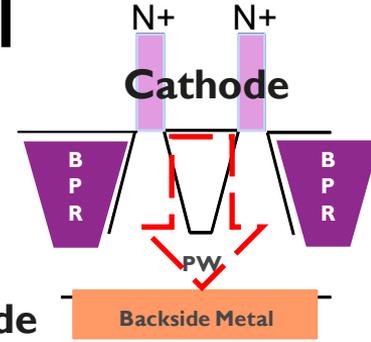
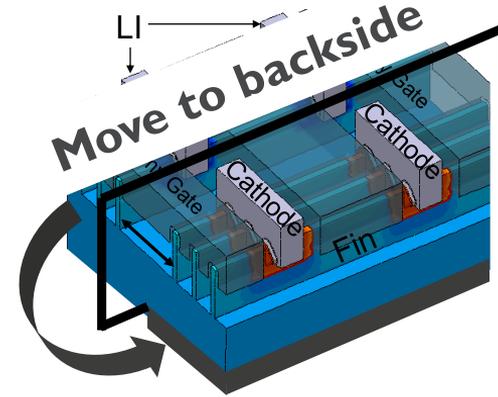
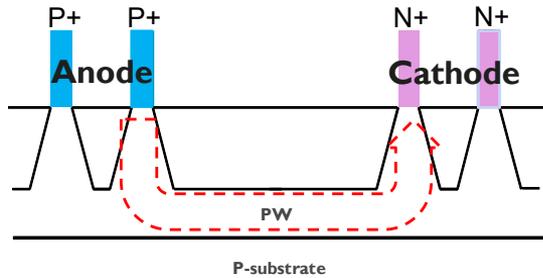
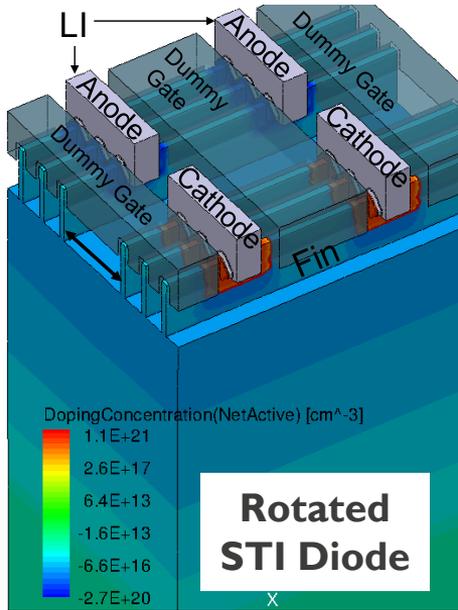
[A. Veloso, VLSI 2022]

"The Transistor: An Indispensable ESD Protection Device – Part 2", InCompliance 2023, <https://incompliancemag.com/the-transistor-an-indispensable-esd-protection-device-part-2/>, accessed 18 August 2024.

Vertical ESD diode

Traditional ESD diode

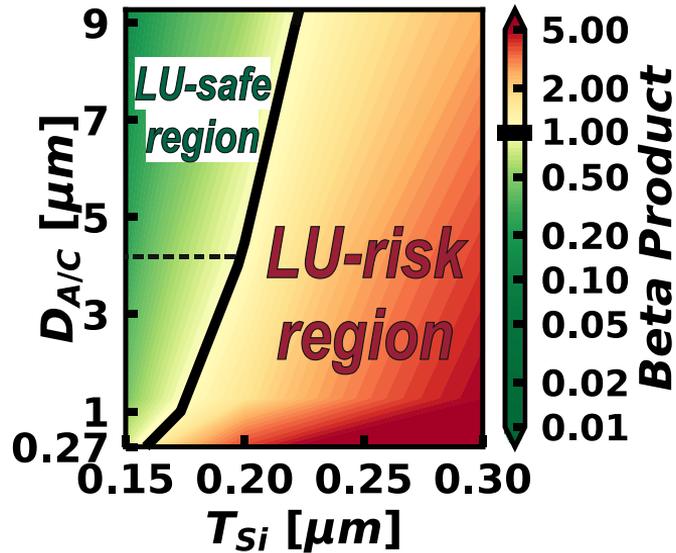
Vertical ESD diode



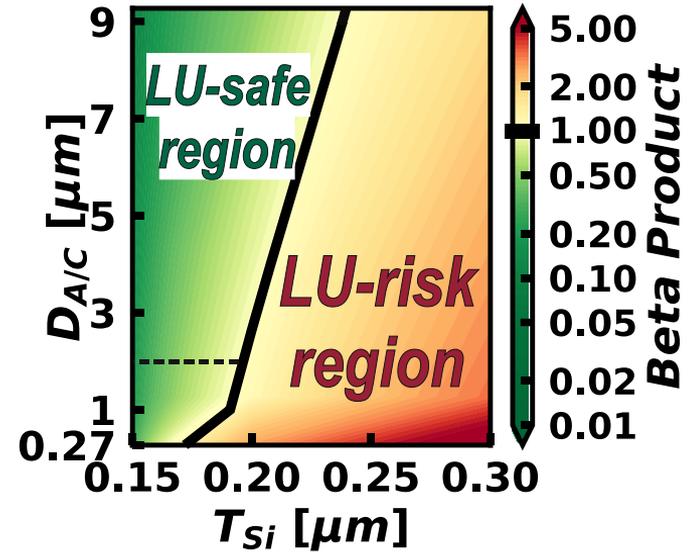
**Proposed ESD diode: layout area reduces ~67%
and I_t^2/area increases 3x**

Thin backside and backside implants reduce latch-up risk!

P+ BS contacts



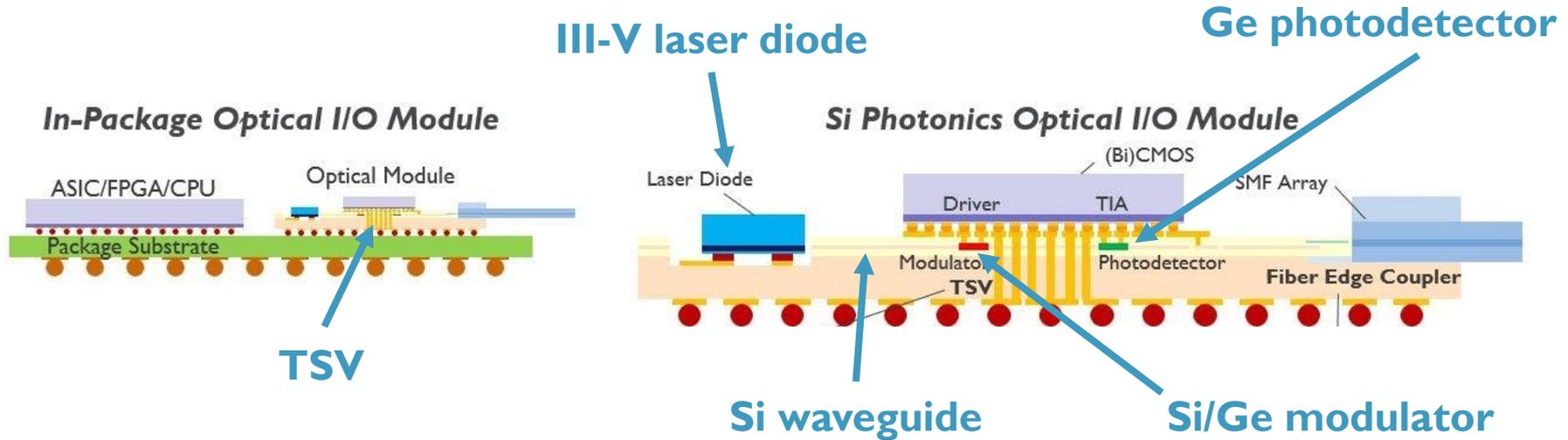
P+ and N+ BS contacts



Optical I/O

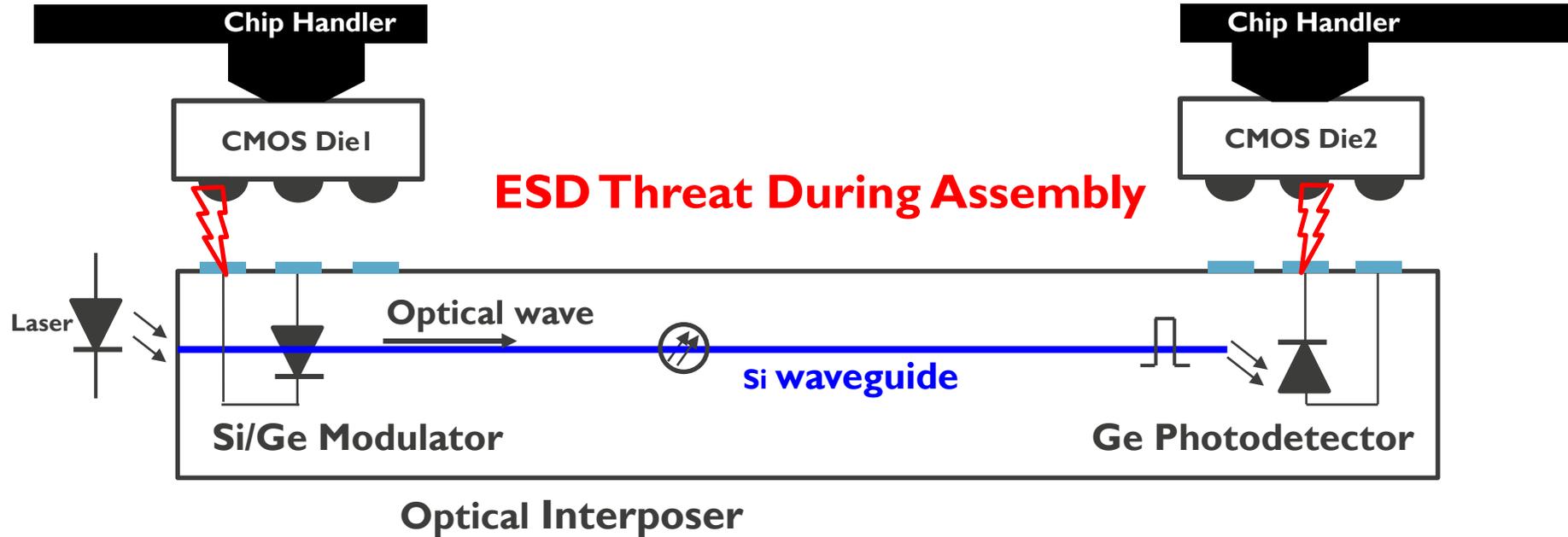
No ESD from optical fibers, right?

“External” communication with “internal” level of ESD protection



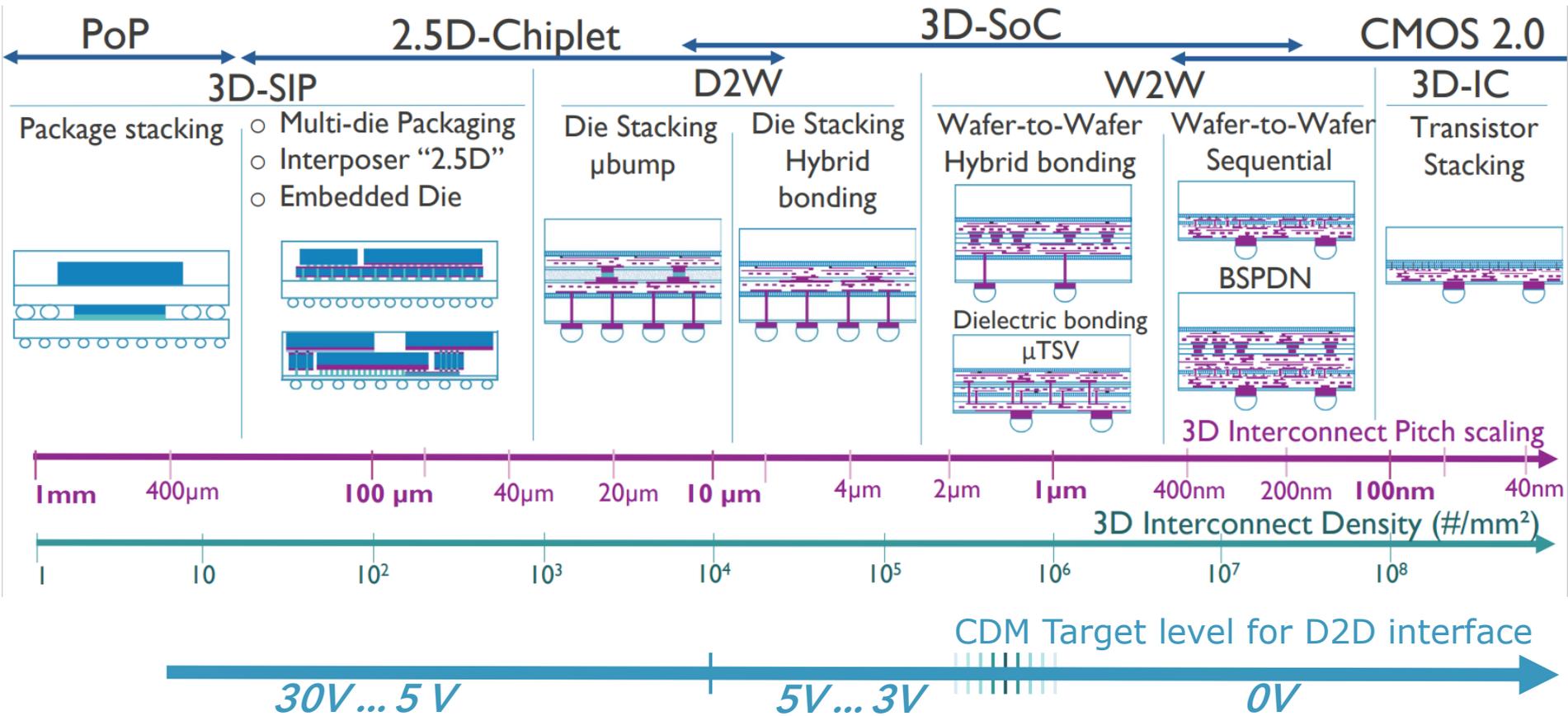
Perfect example of heterogeneous integration!

Optical diodes still need electrical power → ESD risk during assembly

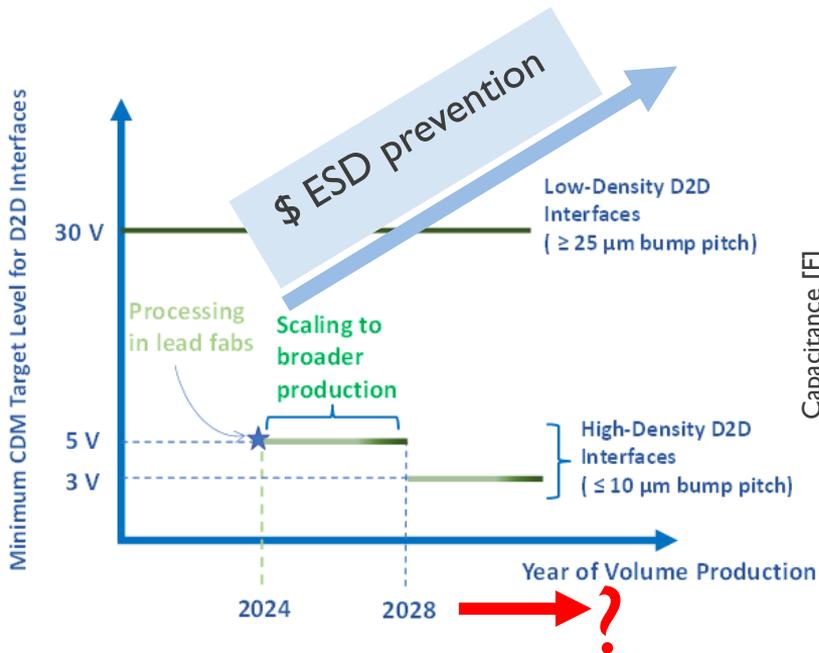


Both OIO and backside connections need
2.5D and 3D interconnect

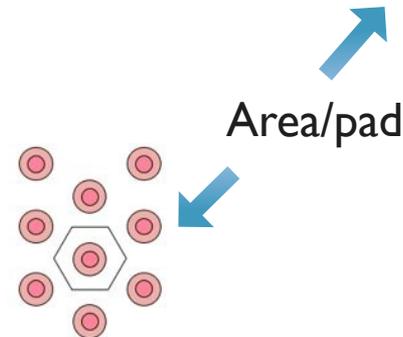
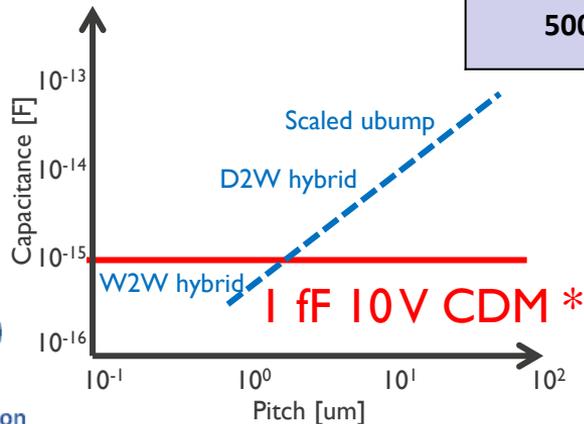
3D interconnect landscape + CDM ESD protection target voltages



ESD protection of every signal pin will be difficult for W2W hybrid bonding, we need to investigate ESD prevention also!



Pitch [nm]	Px	Py	Area [μm^2]
1000	1075	931	1.00
500	537	465	0.25

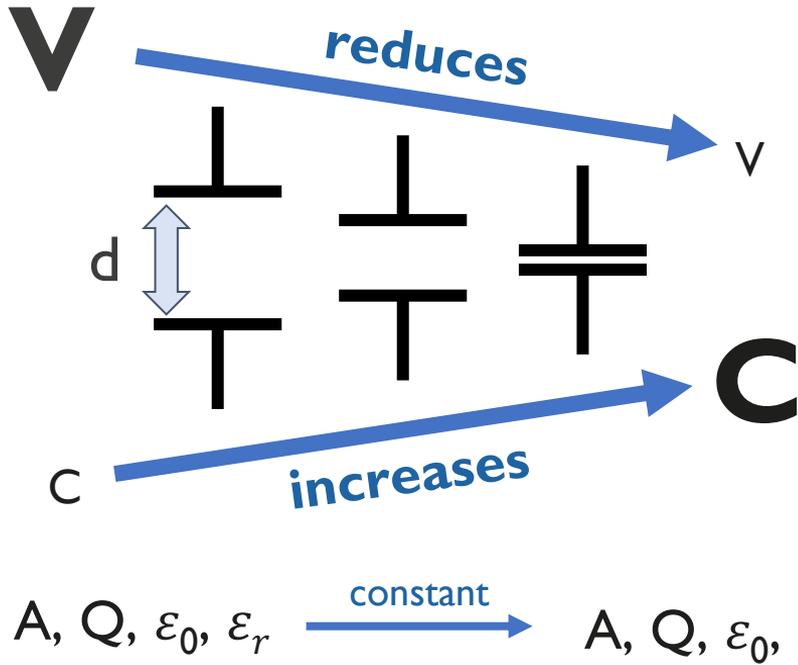


[Industry Council on ESD Target Levels, "White Paper 2-2", 2023]

* [Y-K. Chen IEDM2020]

- The question is how do we meet 5V CDM targeted voltage for stacking technologies?
- Towards 0V CDM ?

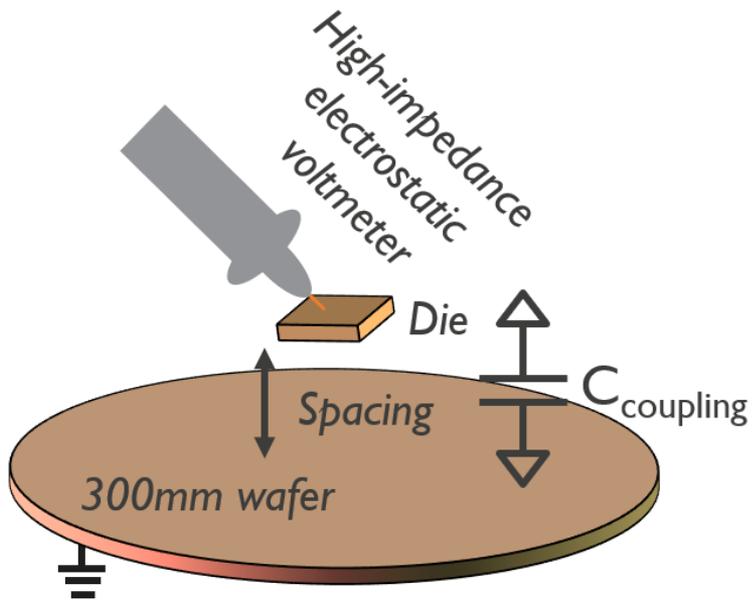
Voltage Suppression Lowers Voltage in Bonding



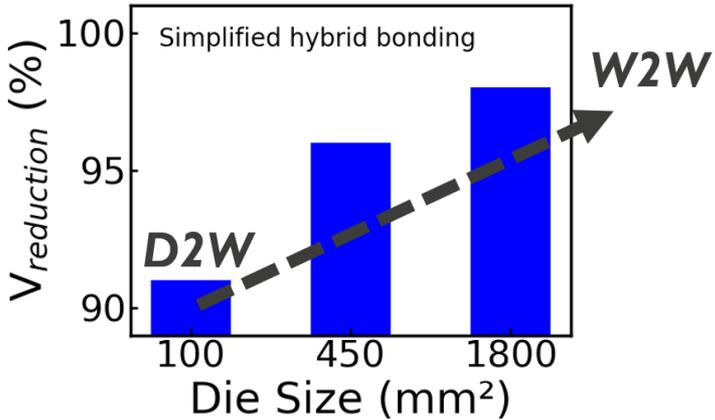
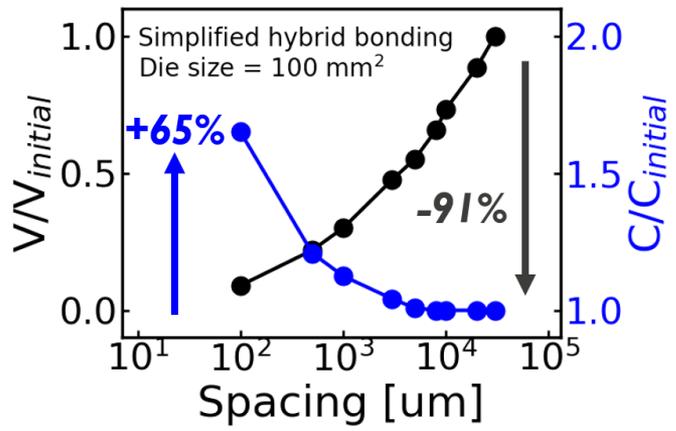
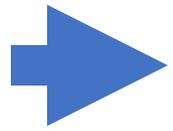
$$C = \frac{\epsilon A}{d} \quad Q = CV$$

Voltage suppression effect:
 $W2W > D2W$

W2W Bonding shows Superior Voltage Suppression



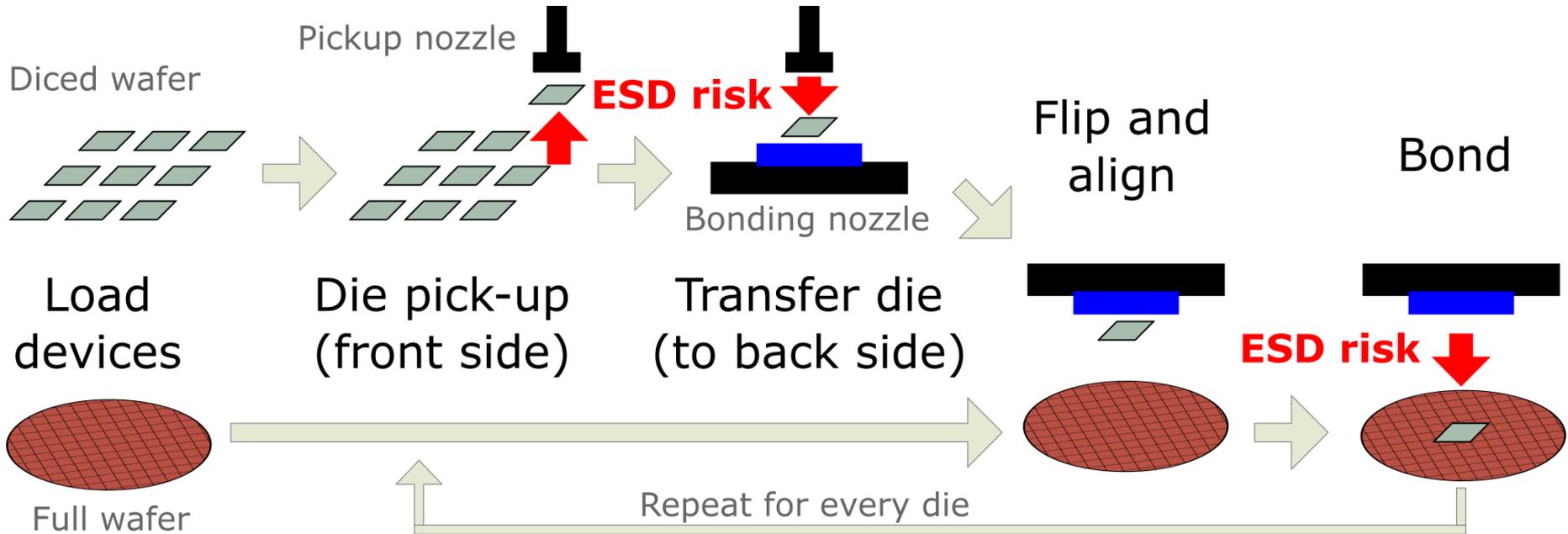
- D2W: \uparrow 65% in $C_{coupling}$ and \downarrow 91% in V
- Voltage suppression : **W2W > D2W**



[S. Lin et al. VLSI Symposium 2024]

ESD control and bonding process assessment
becomes more important than ever

Die-to-wafer (D2W) bonding process assessment



ESD control process assessment becomes essential in adv. bonding

- Installing an ionizer is not enough to guarantee 5V and 3V CDM
- Only way to guarantee ESD safety is customiyed prevention!

ANSI/ESD SP17.1-2020



*For the Protection of Electrostatic
Discharge Susceptible Items –*

Process Assessment Techniques

*Electrostatic Discharge Association
7900 Turin Rd., Bldg. 3
Rome, NY 13440*

*An American National Standard
Approved December 15, 2020*

ANSI/ESD SP17.1-2020

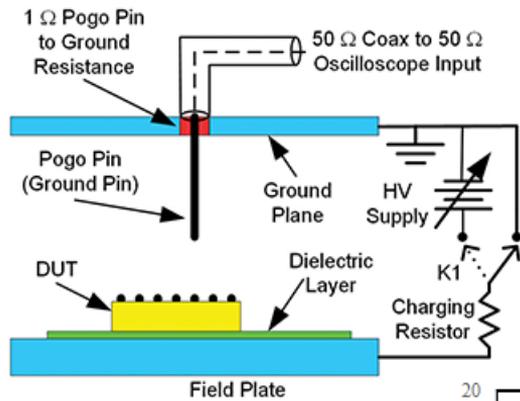
ESD Association Standard Practice

Testing ESD will change fundamentally

Shrinking bonding pads will make direct testing impossible

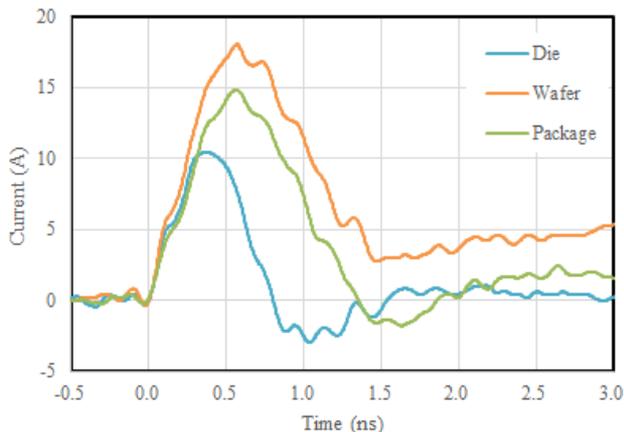
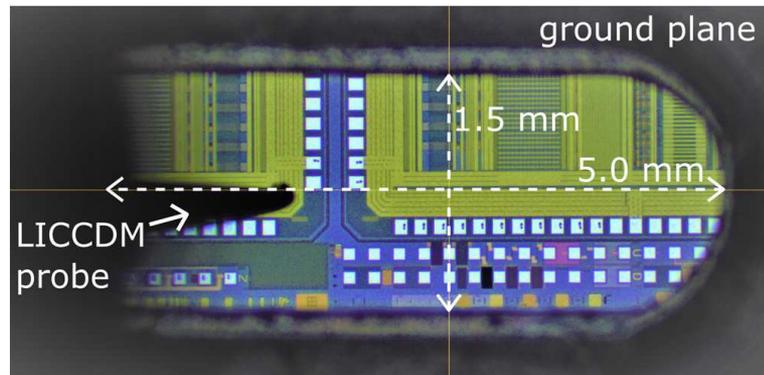
Field-induced-CDM (JS-002 standard)

Package-level test

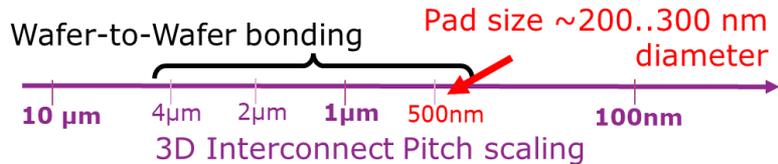


Contact CDM (no standard)

Bare die/wafer-level test



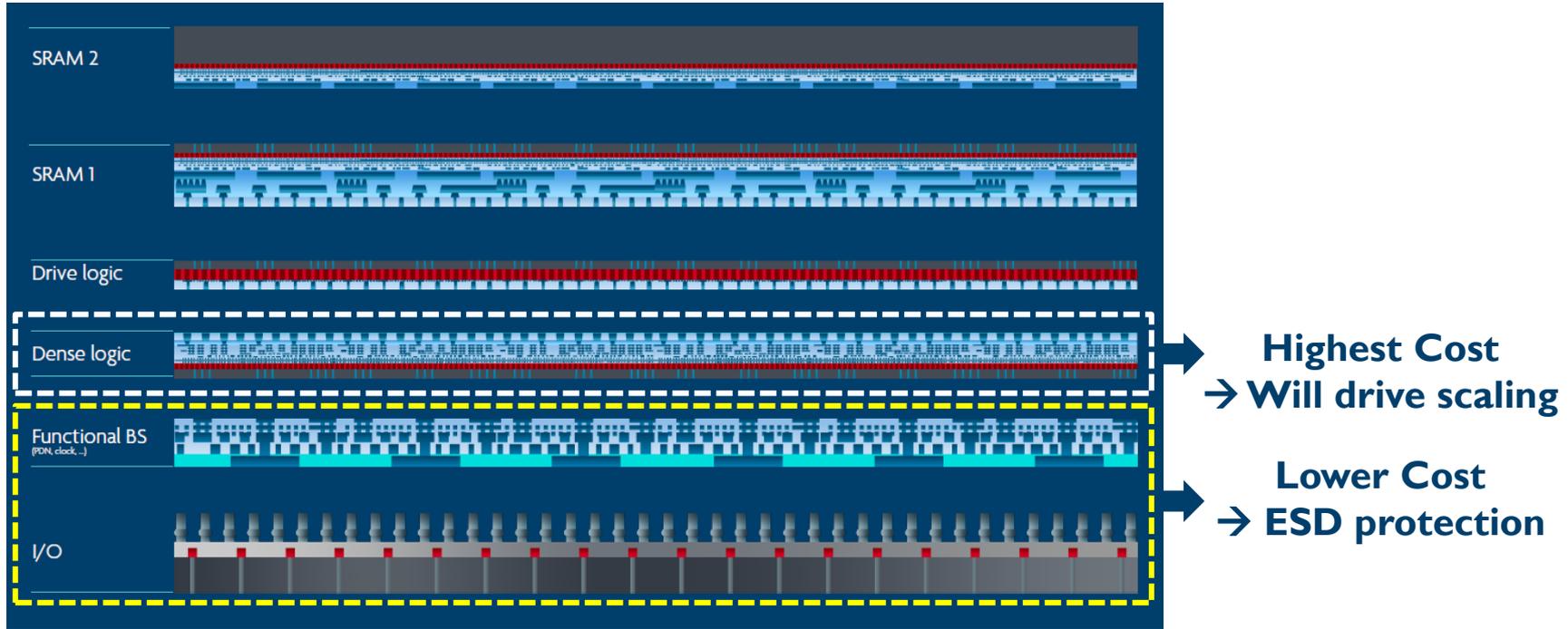
Sub-ns pulse width!



T. Suzuki et. al, EOS/ESD Symp. 2019.
M. Simicic et. al, EOS/ESD Symp. 2021.

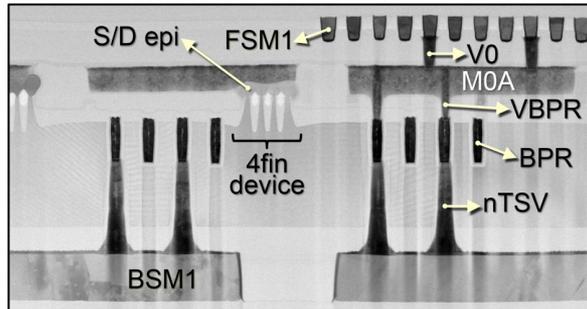
Bringing it all together

It's all about rearchitecting towards a smart partitioning (CMOS 2.0)

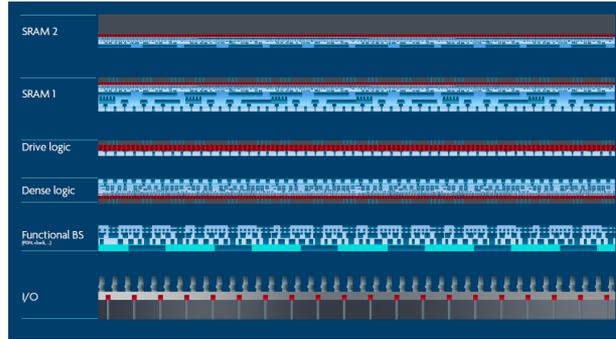


**Same 'look & feel' as a classical CMOS platform
But offering versatility for System optimization**

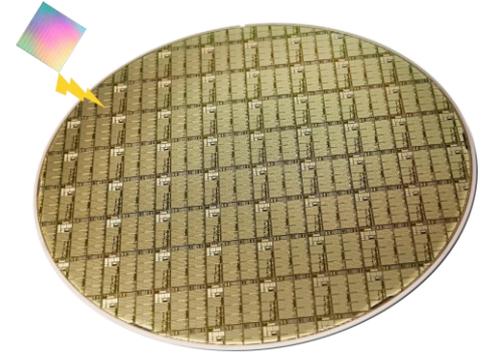
Conclusions



- Si bulk is disappearing
- Creates opportunity for vertical diode



- Technologies become more function-specific
- ESD protection can move back to old tech.



- Reusability of chiplets is needed to reduce price
- Standardization is a must !

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- Imec DTCO program and partners

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