Programirljivi logički sklopovi (FPGA) u praktičnoj nastavi

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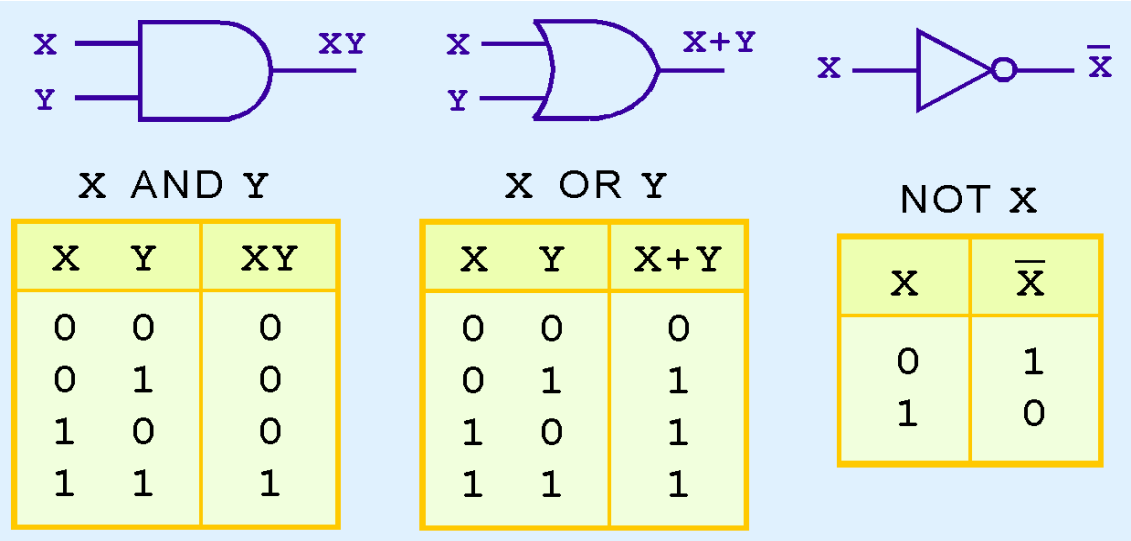
IEEE obrazovanje @ FER 2015.

Sadržaj predavanja

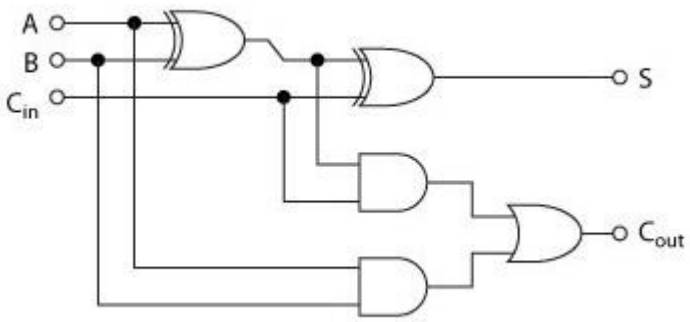
- Cilj: unaprijediti praktičnu nastavu
  - demistificirati teoriju kroz opipljive primjere
  - poticati samostalni rad i eksperimentiranje
- Programirljivi logički sklopovi: sredstvo
  - FPGA tehnologija
  - logistika (~400 / 750 studenata)
- Laboratorijske vježbe
  - demo!
- Učinak, otvorena pitanja
- Diskusija

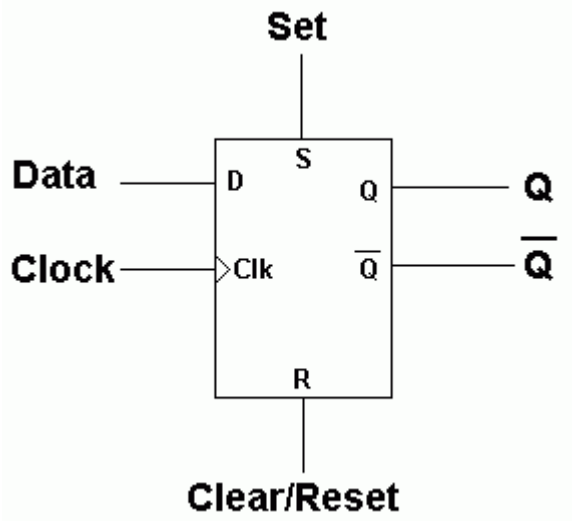
Logički sklopovi i Booleova algebra: temelj digitalnog doba

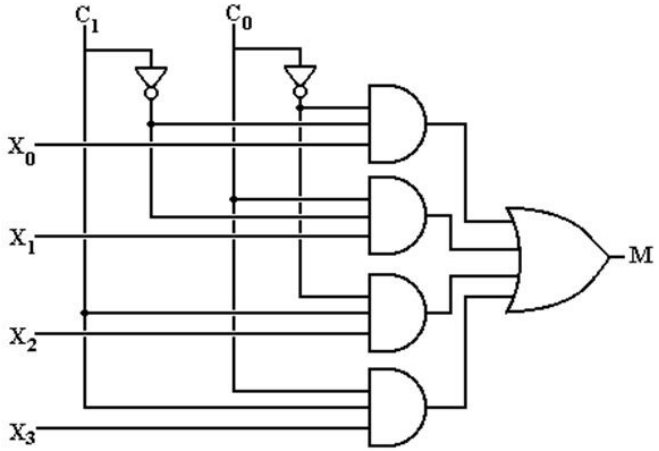


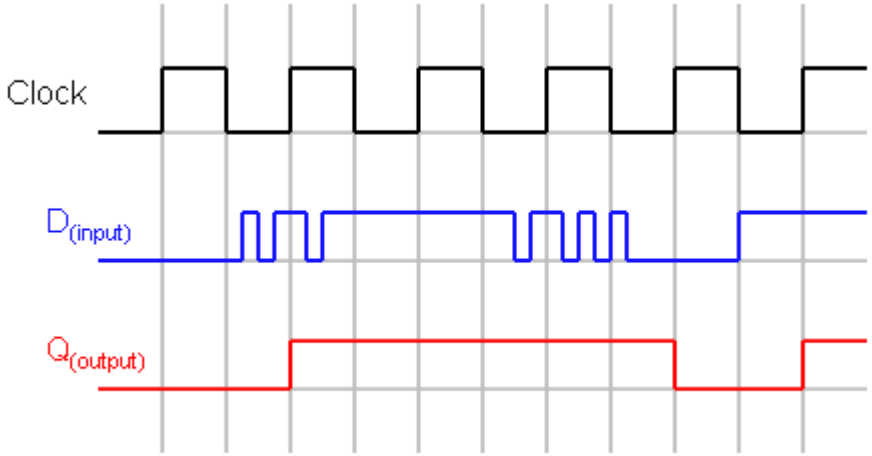
- Digitalna logika @ FER-2: obavezni kolegij na 1. godini
- Cilj: *upoznati studente s temeljnim principima izgradnje digitalnih sustava ... obradit će se osnovni kombinacijski i sekvencijski elementi i moduli, kao i način ugradnje digitalnih sustava u stvarni svijet.*

Kombinacijski i sekvencijski sklopovi

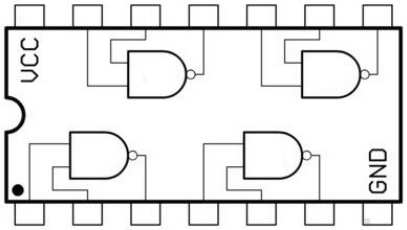


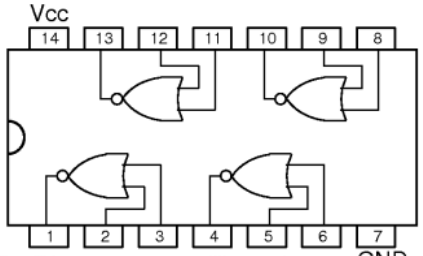


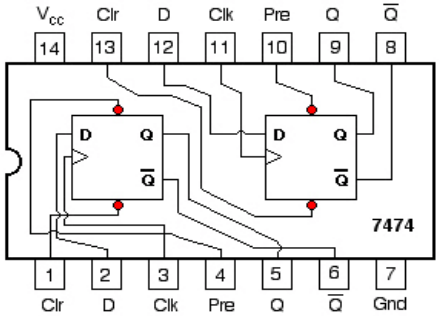


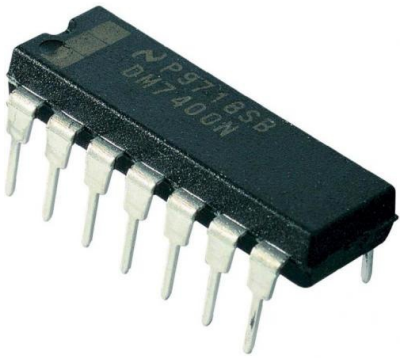


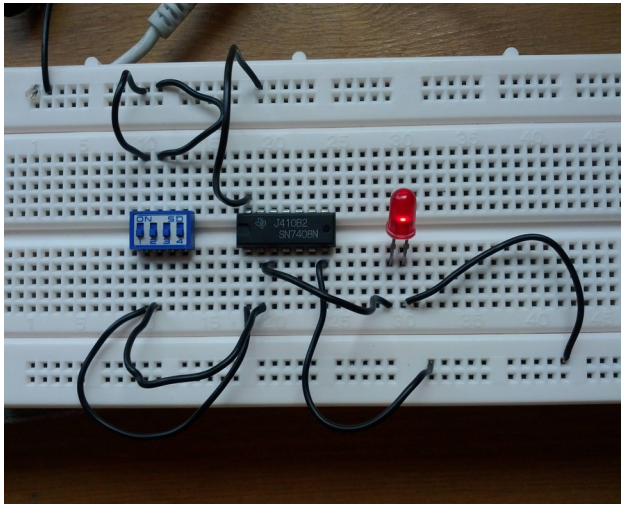
Prototip digitalnog sklopa: nekad...

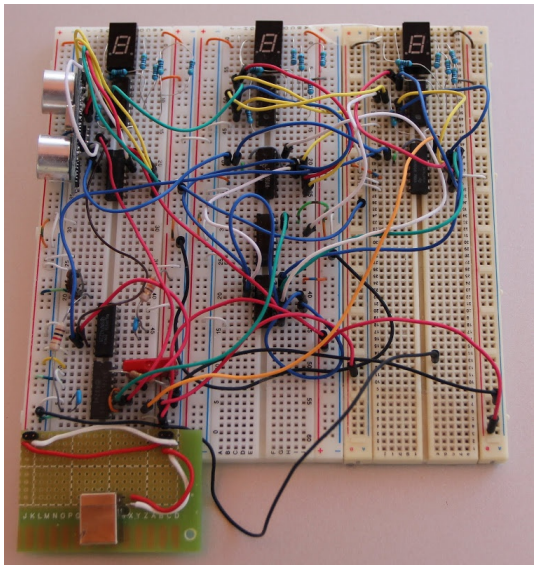


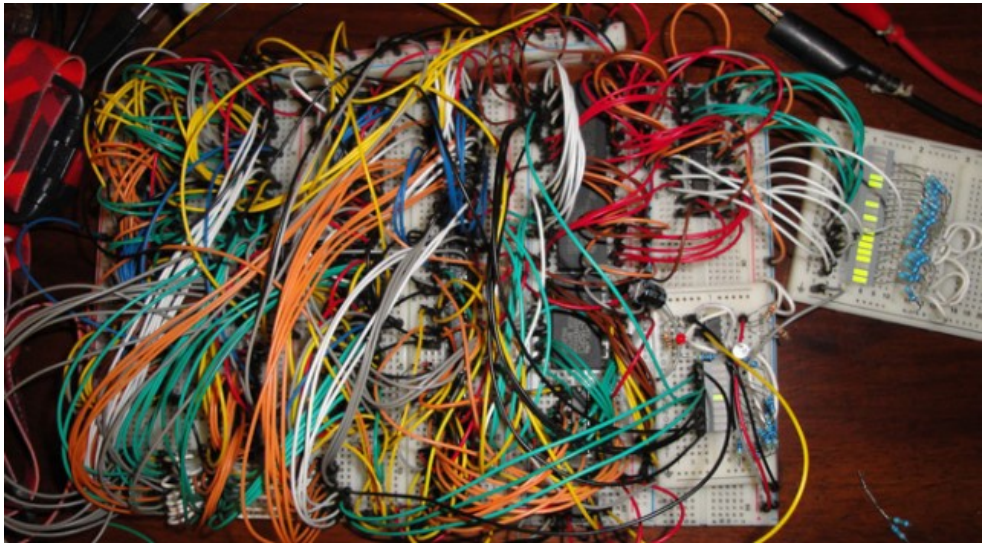




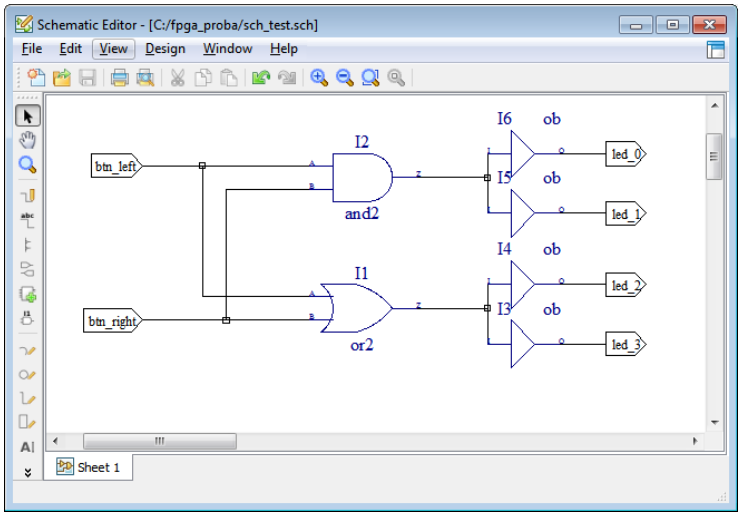


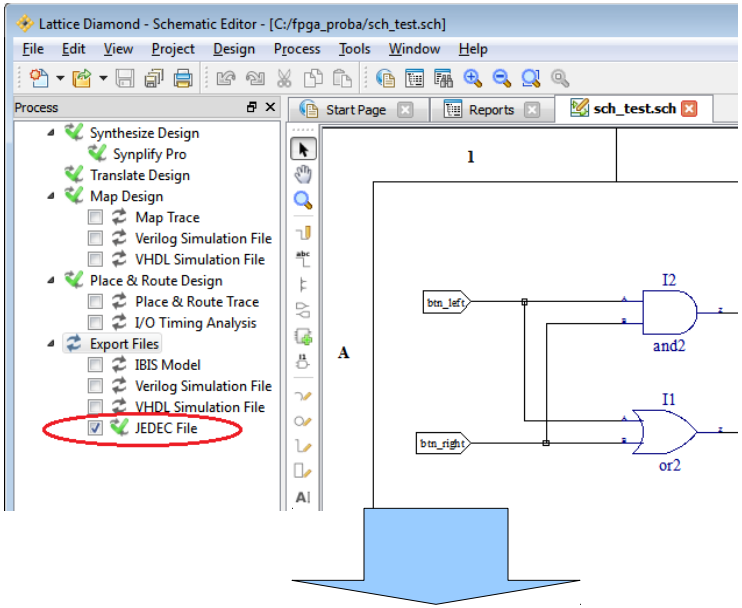




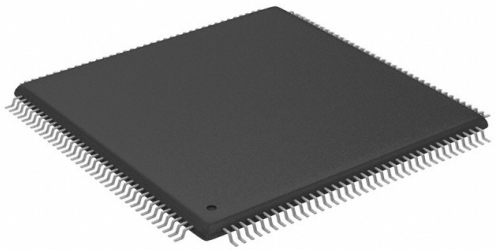


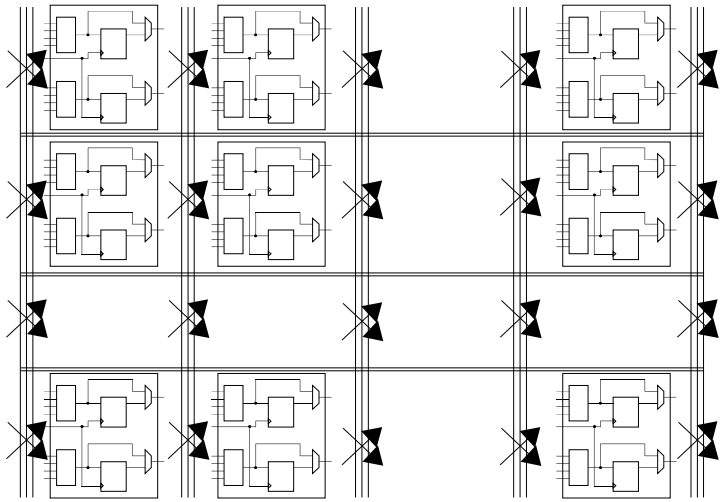
Prototip digitalnog sklopa: ... i danas



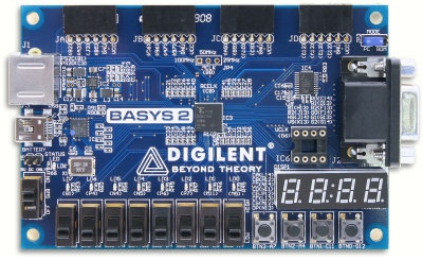


Field
Programmable
Gate
Array





Komercijalne FPGA razvojne platforme

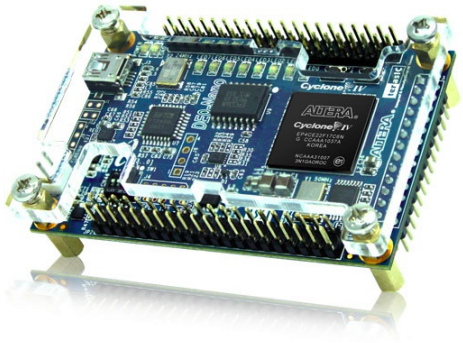


89 USD

1099 USD

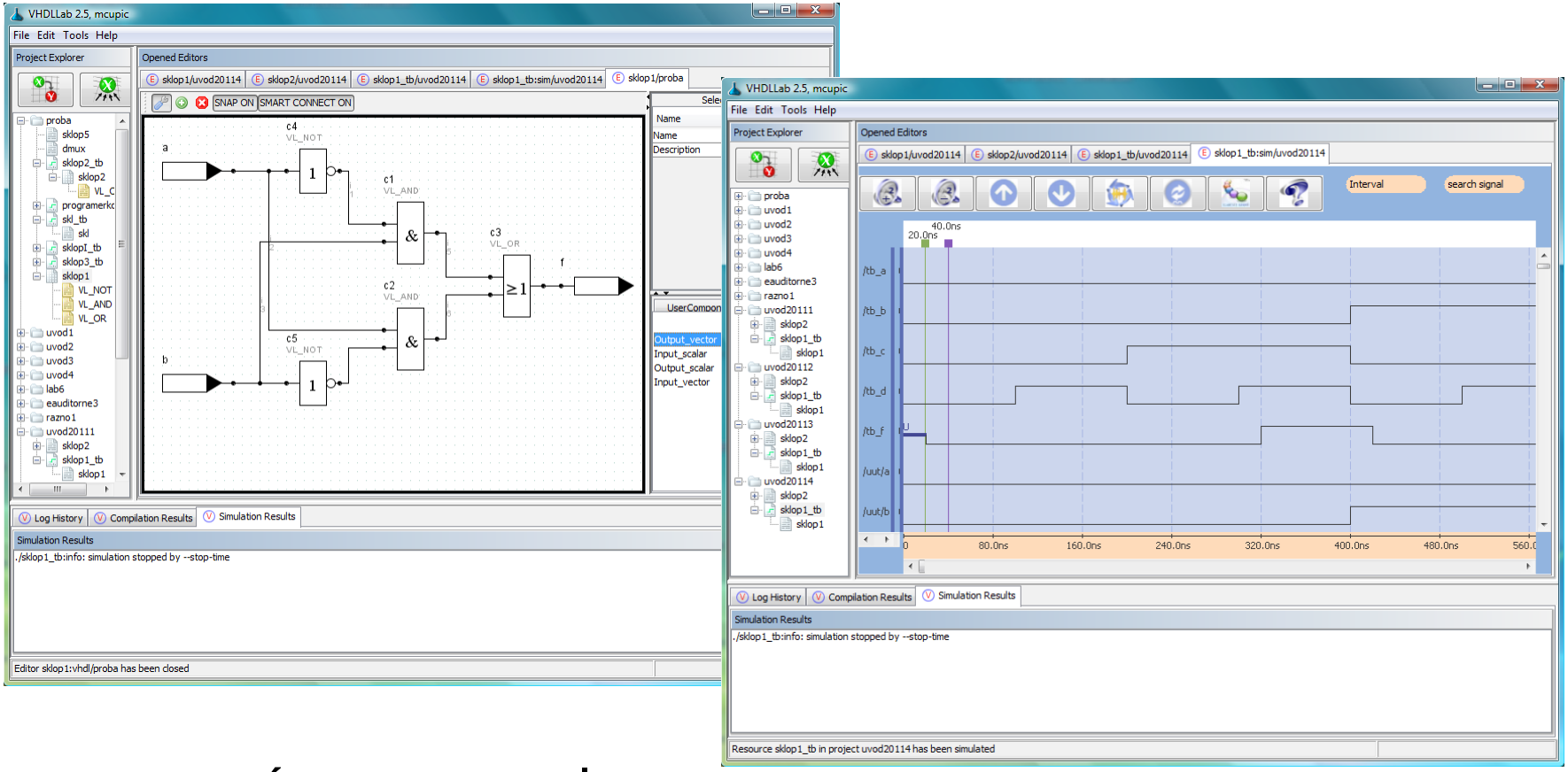
69 USD

79 USD



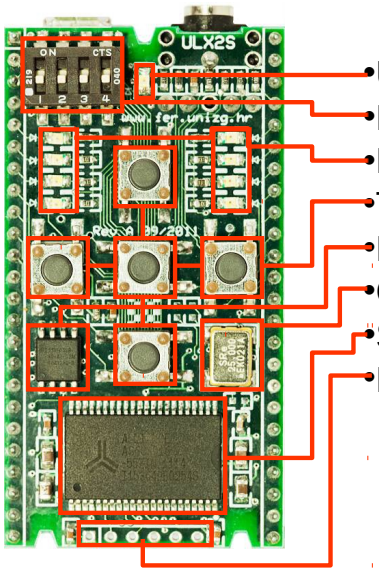
- Problem: cijena opremanja laboratorija (nekad)
- Problem: održavanje ispravnosti (400 .. 800 studenata)
- Problem: strah od kvara: kreativnost--
- Problem: vremensko ograničenje (2 h/vj): kreativnost--
- Rješenja?

Vlastiti razvoj: VHDLLab (simulacijski alat)

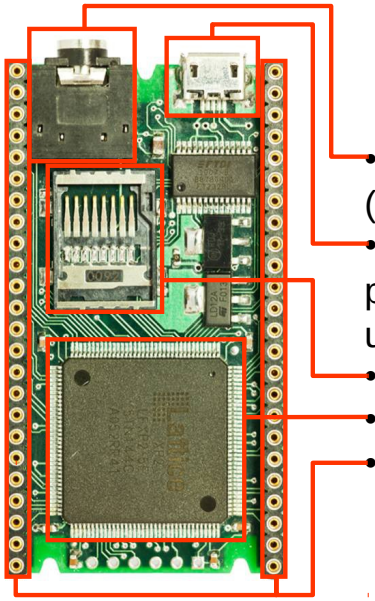


- omogućen samostalan rad (od kuće)!
- dijelu studenata (pre)visoka razina apstrakcije

Vlastiti razvoj – FPGA sklopovska platforma



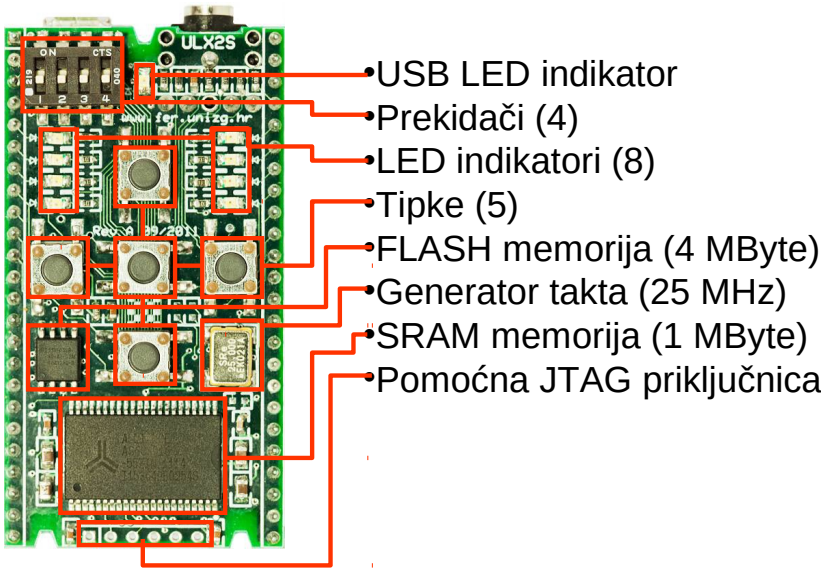
- USB LED indikator
- Prekidači (4)
- LED indikatori (8)
- Tipke (5)
- FLASH memorija (4 MByte)
- Generator takta (25 MHz)
- SRAM memorija (1 MByte)
- Pomoćna JTAG priključnica

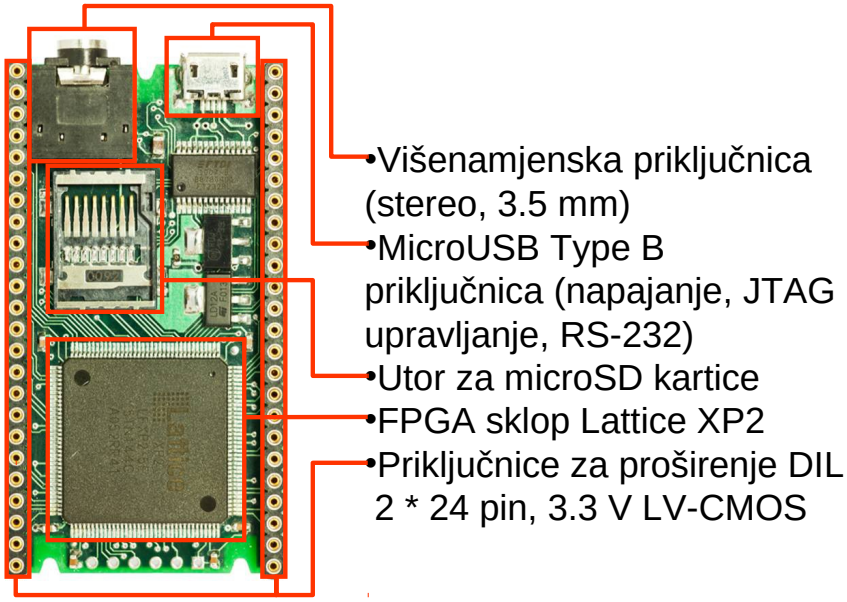


- Višenamjenska priključnica (stereo, 3.5 mm)
- MicroUSB Type B priključnica (napajanje, JTAG upravljanje, RS-232)
- Utor za microSD kartice
- FPGA sklop Lattice XP2
- Priključnice za proširenje DIL 2 * 24 pin, 3.3 V LV-CMOS

- FER – RIZ-Odašiljači – Skriptarnica
  - proizvedeno u Hrvatskoj! (cca. 500 kom.)
- 316 kn (~42 USD + PDV) za studente
- FPGA: Lattice XP2, 8000 LUT
- Napajanje i programiranje putem USB-a

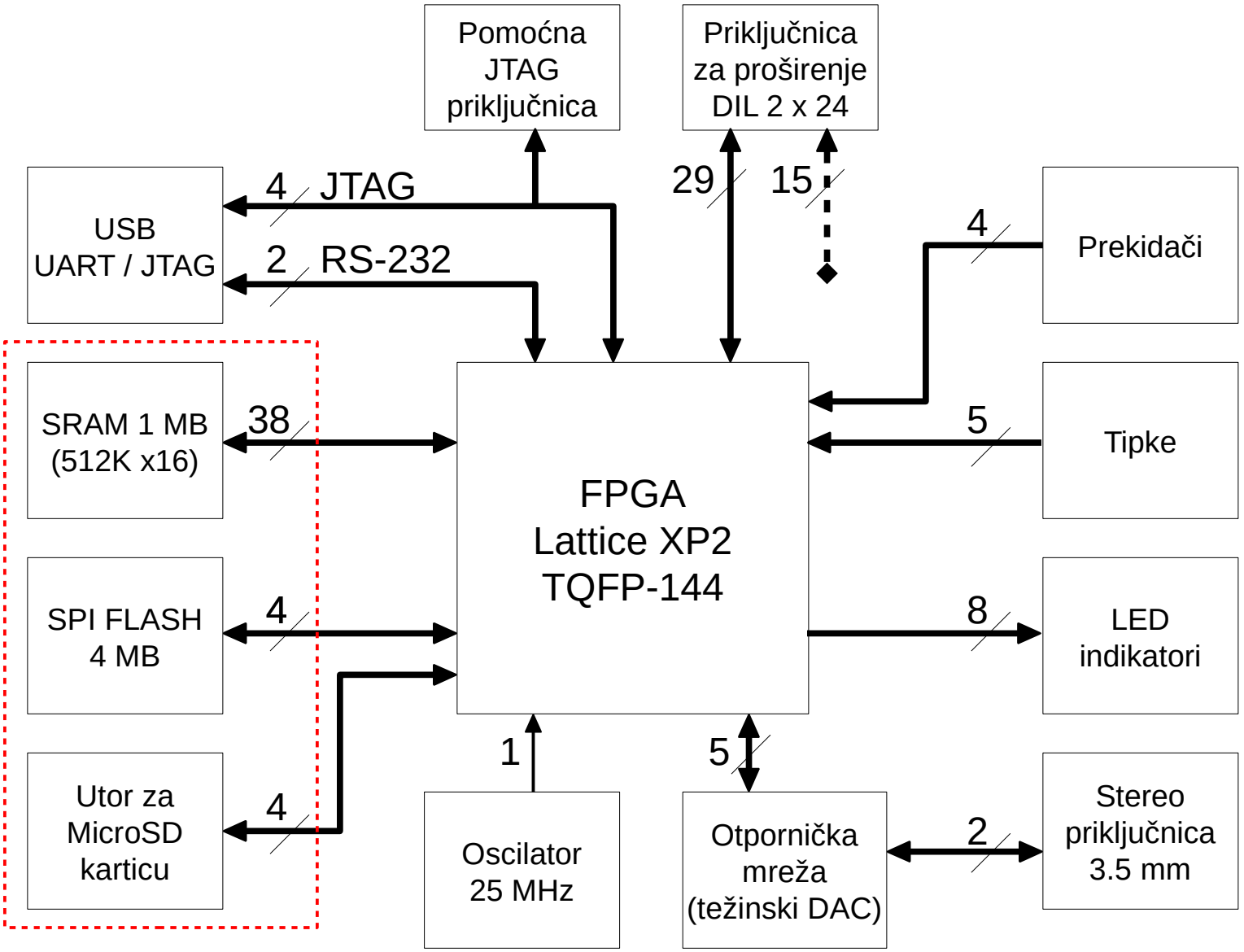
Nova paradigma laboratorijske logistike



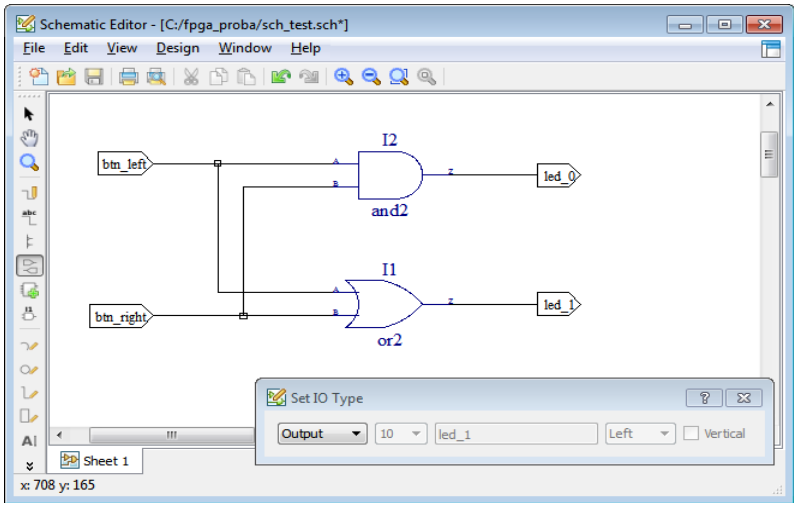


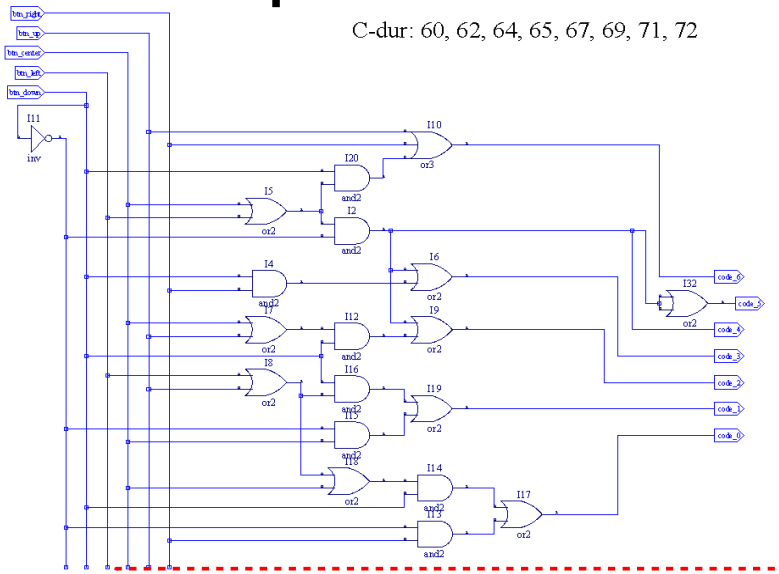
- studenti sami nabavljaju (i čuvaju!) pločicu
- omogućen samostalan rad kod kuće, u trajanju i u vrijeme koje studentu najbolje odgovara
- otvorena mogućnost samostalnog eksperimentiranja, kao i primjene u drugim kolegijima
- teret logistike prebačen na dobavljača i studente :)

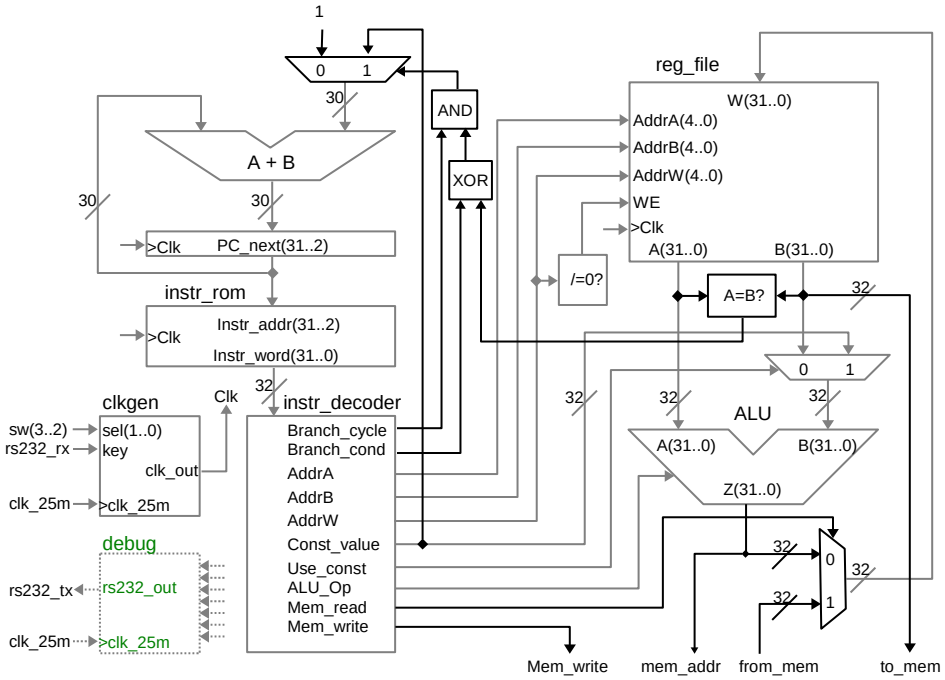
Razvojna pločica ULX2S – blok shema

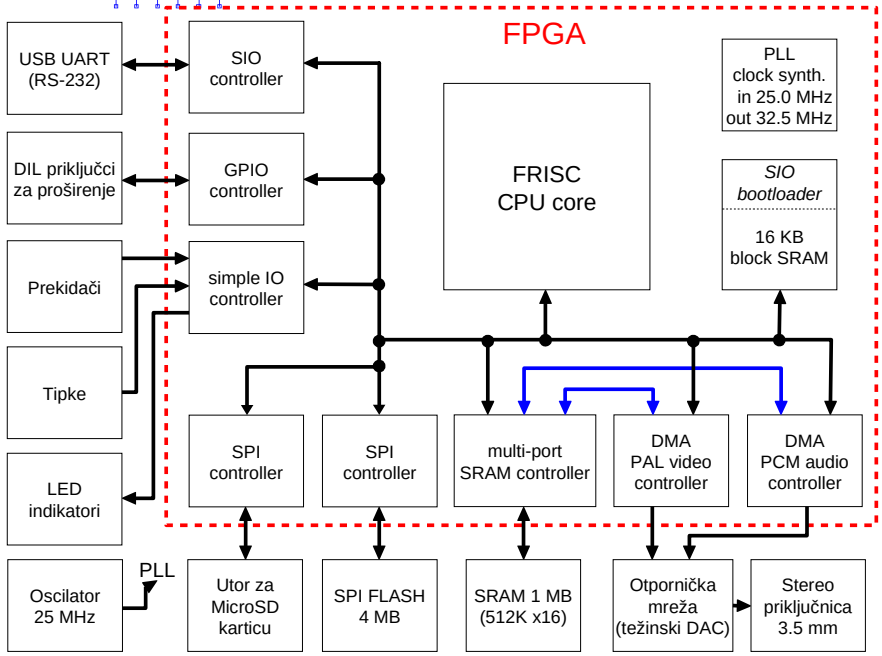


Od elementarne logike do mikroprocesora









Digitalna logika: laboratorijske vježbe

- Uvodna vježba
  - shematski opis sklopa, daljinski upravljač makete
- Kombinacijski sklop za sviranje
  - shematski opis, primjena K-tablica
  - opis VHDL-om
- Aritmetički kombinacijski sklopovi
  - ALU, registri
- AFSK modem
  - brojila, ROM, D-A pretvorba
- Automati
  - upravljač semafora
  - vođenje radioupravljive makete

DEMO!

Učinak, otvorena pitanja

- Ispunjena očekivanja:
  - studenti u kontaktu s opipljivim hardwareom
  - (djelomično) demistificirana FPGA tehnologija
  - veći angažman studenata na labosima
  - samostalni studentski i vanjski projekti
    - LEGO roboti, servo PWM, LCD driver...
    - “portovi” 8-bitnih igraćih konzola (z80 / 6502)
- Upitni rezultati:
  - varijanta lab. vježbe (simulacijska / sklopovska) ne utječe na ishod provjera znanja
  - samostalno eksperimentiranje ispod (možda nerealnih) očekivanja

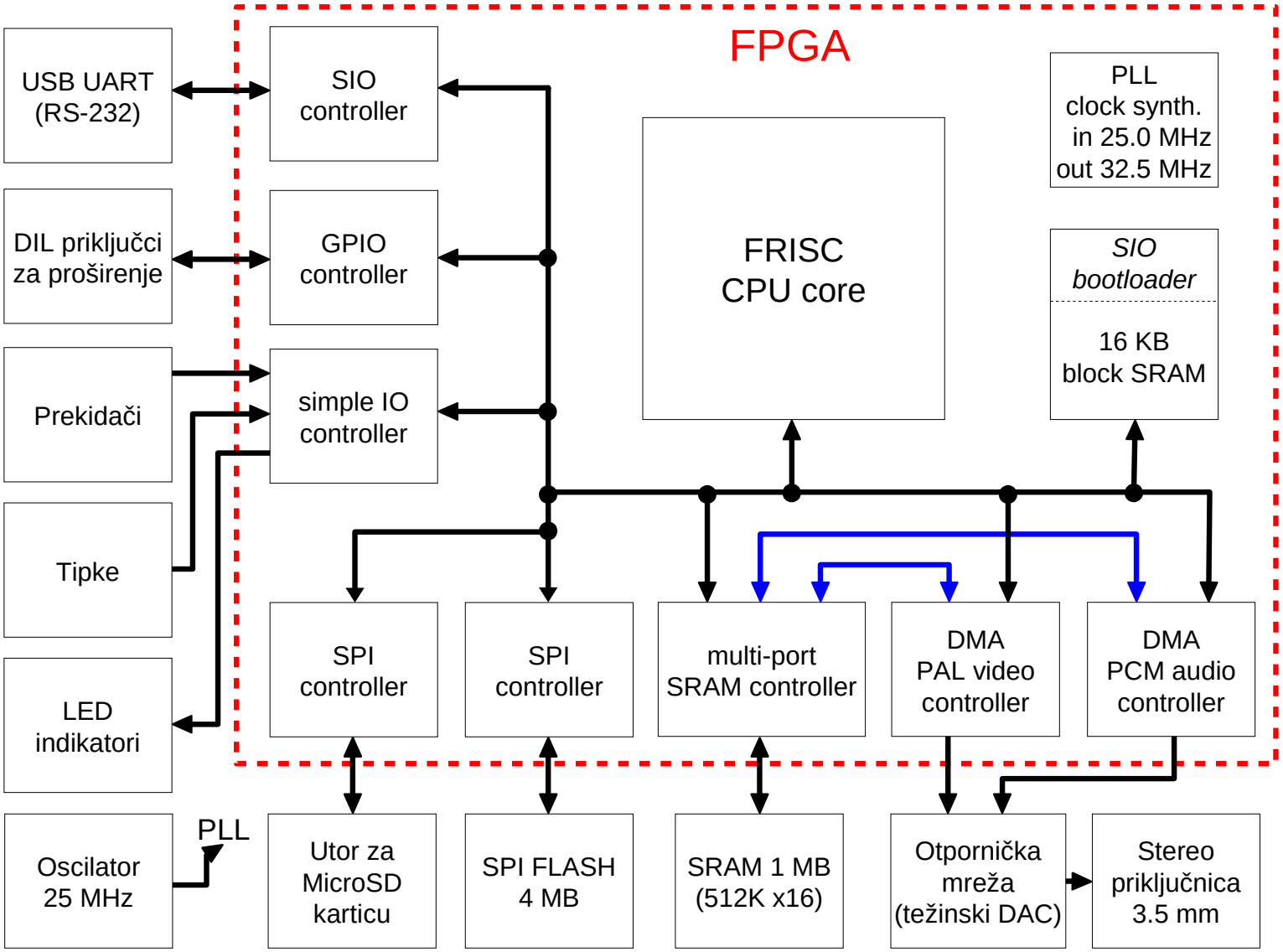
Učinak, otvorena pitanja

- FER (2011, dekan prof. Perić) – osigurao materijal za izradu prototipne serije
- RIZ Odašiljači d.d. - donirali trošak pripreme SMD stroja i montaže dosadašnih serija pločica
- Skriptarnica – investitor i nositelj rizika proizvodnje i plasmana dosadašnjih serija

- Proizvodnja većih serija – manja cijena?
- Primjena izvan okvira temeljnog kolegija?
  - mikroprocesorski sustav – python, BASIC, C, asm...
- Primjena izvan akademskog okruženja?

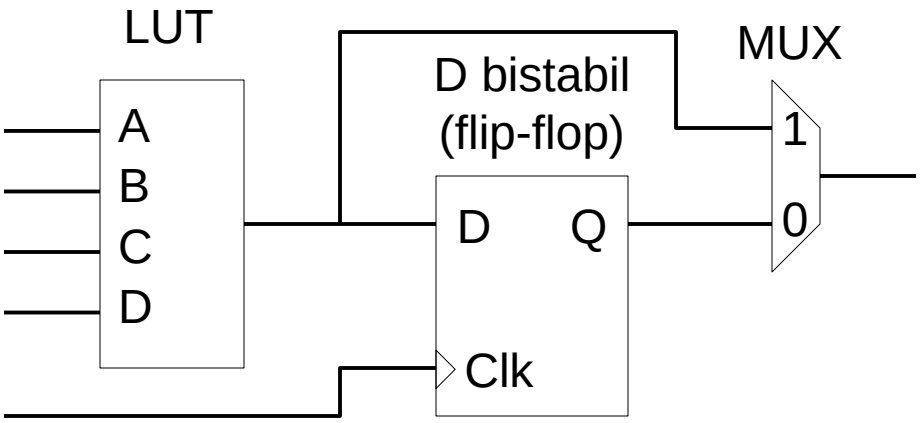
http://www.nxlab.fer.hr/dl

FRISC (FER RISC) system-on-a-chip



FPGA – *field programmable gate array*

- hrv. *programirljivo polje logičkih blokova*
- temeljni logički blok sastoji se od
  - pregledne tablice (lookup table)
    - kombinacijski element
  - bridom okidanog D-bistabila (D flip-flop)
    - sinkroni memorijski element



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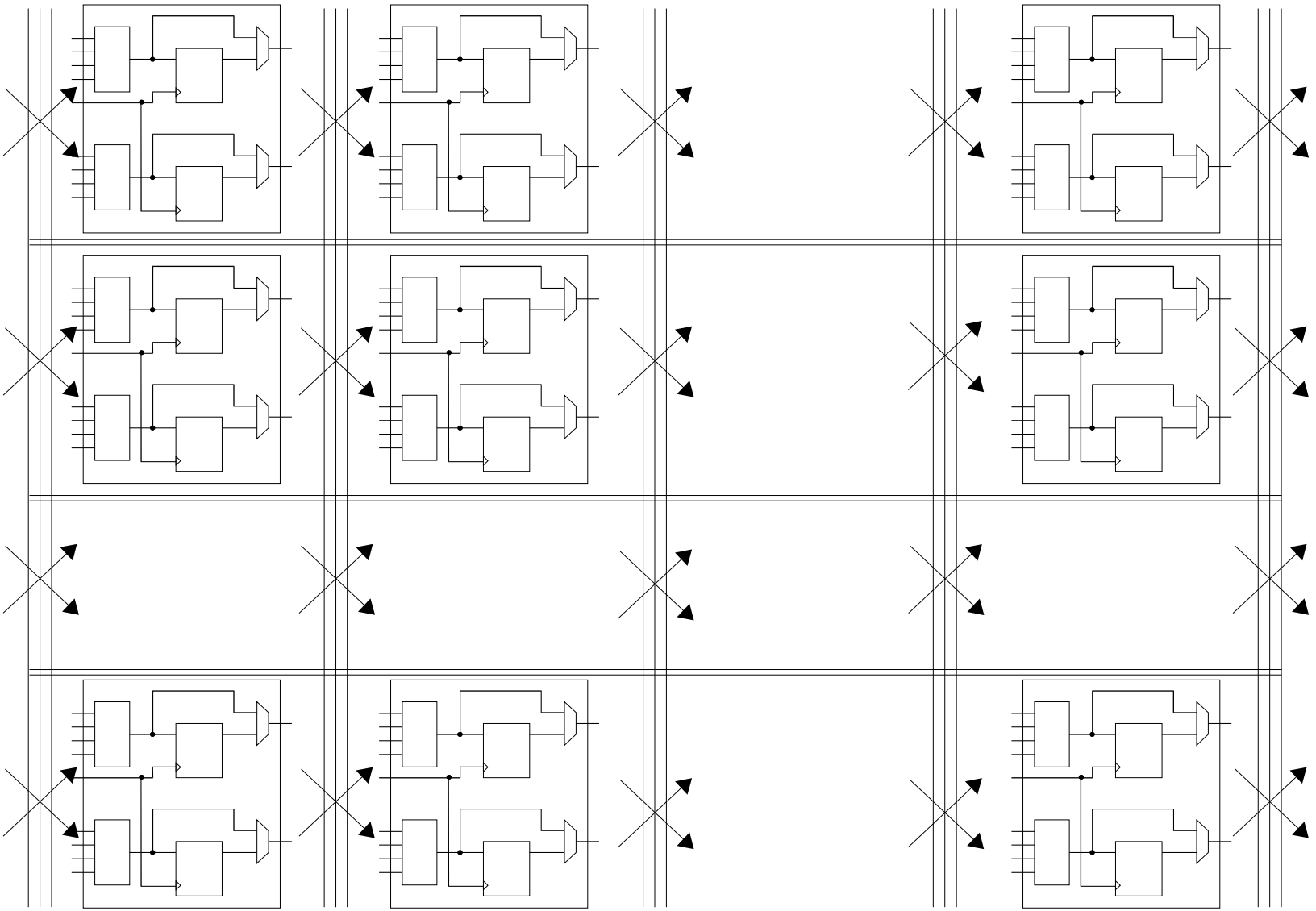
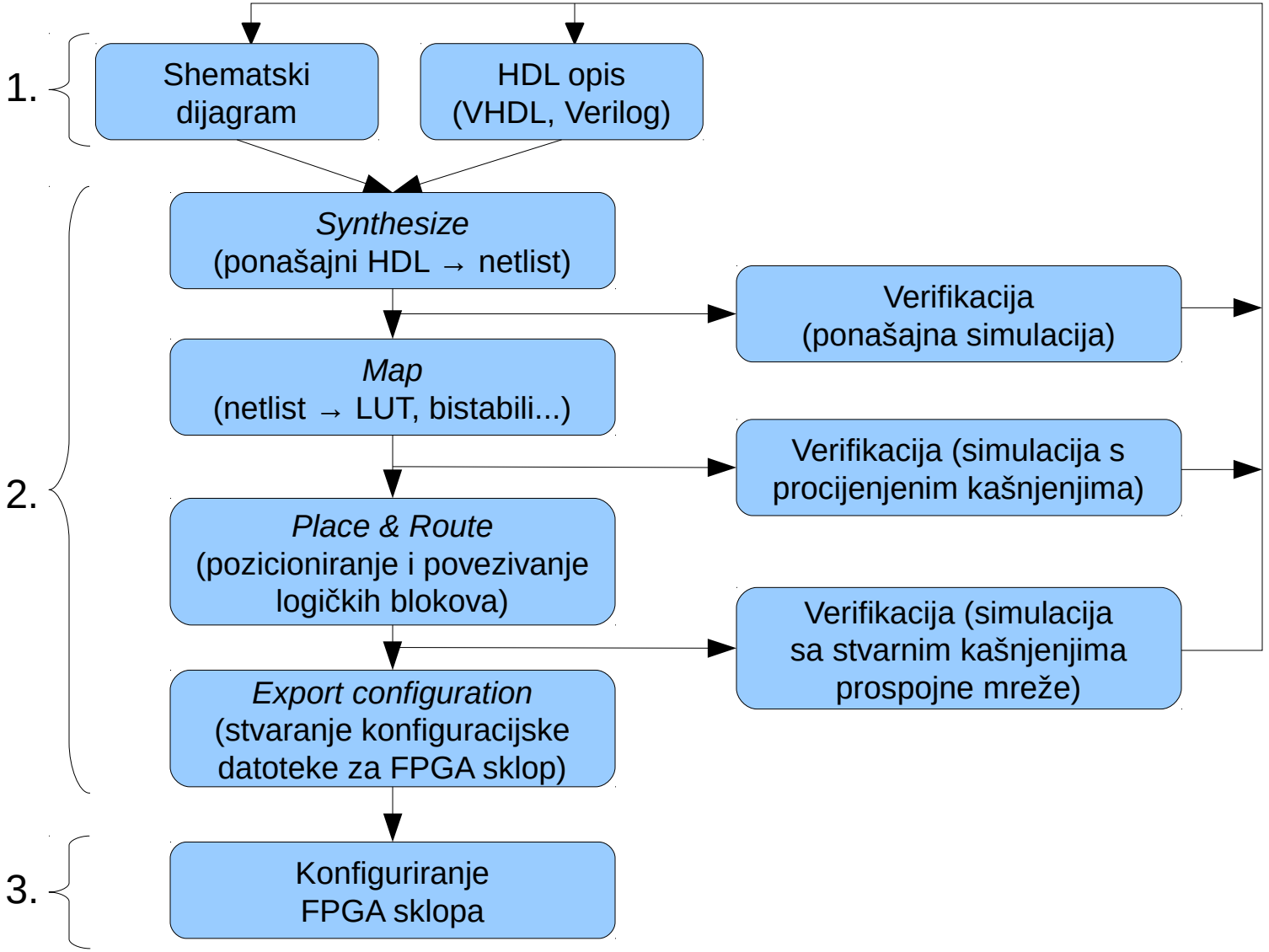
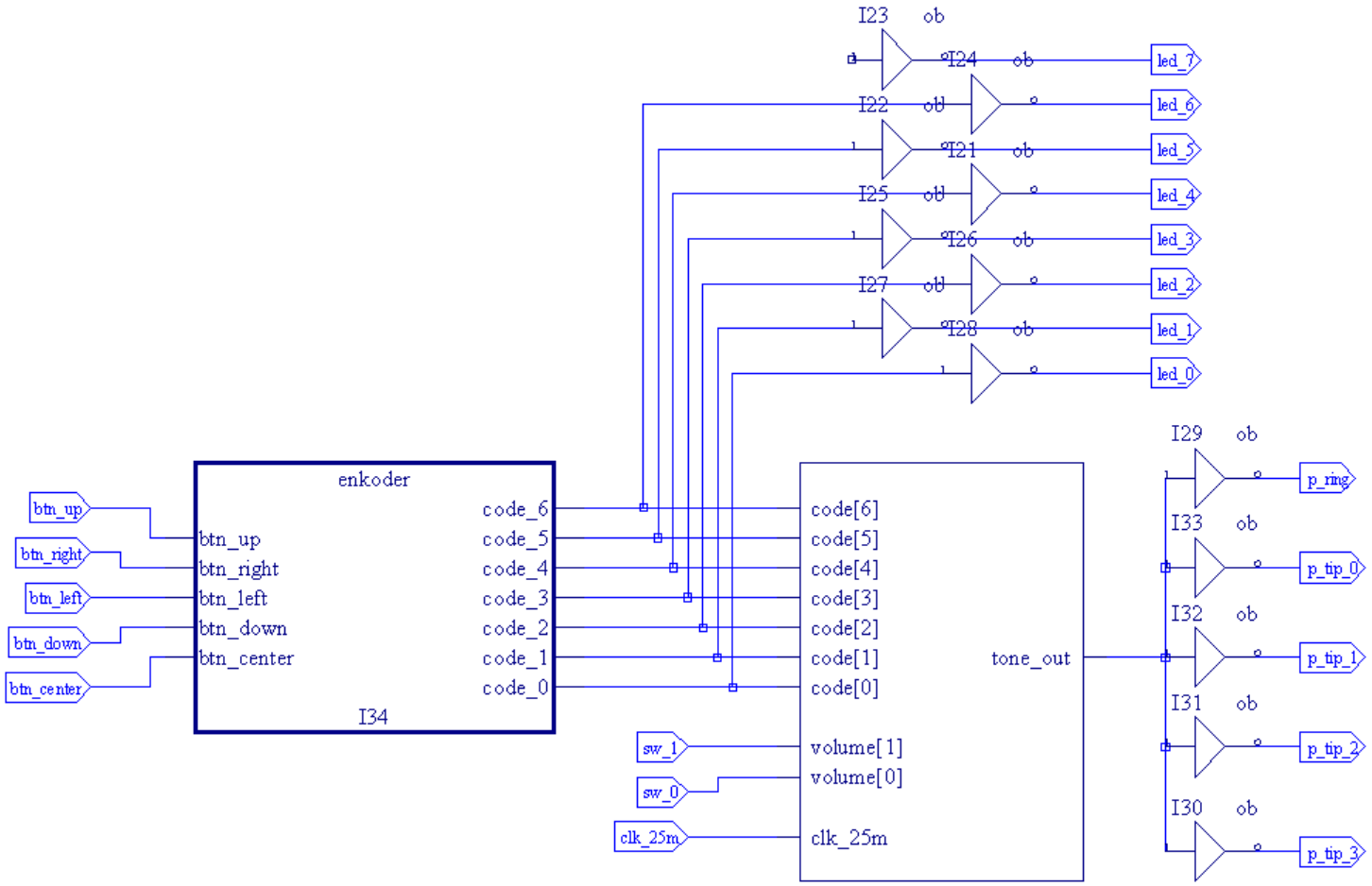


FPGA *design flow*



Primjer nove lab. vježbe na DL: sviralica (blok shema)



Primjer nove lab. vježbe na DL: sviralica (enkoder tipke -> MIDI)